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p. 381

Proceedings: Computer Science and Data Systems Technical Symposium Volume 2

NASA
ANALYTIC
(1 + 24)
IN-CAT. 61-TM
DATE
OVERRIDE

Date for general release August 1987

Proceedings of a symposium held at the
Xerox Training Center
Leesburg, Virginia
April 16-18, 1985

(NASA-TM-89286) PROCEEDINGS: COMPUTER SCIENCE AND DATA SYSTEMS TECHNICAL SYMPOSIUM, VOLUME 2 (NASA) 381 p Avail: NTIS HC A17/MF A01 CSCL 09B
N87-29144
--THRU--
N87-29169
Unclas
G3/61 0093277

	2. Government Accession No.	3. Recipient's Catalog No.

Title and Subtitle Proceedings: Computer Science and Data Systems Technical Symposium, Volume 2	5. Report Date August 1985 6. Performing Organization Code RC
Author(s) Ronald L. Larsen and Kenneth Wallgren, Co-Chairmen	8. Performing Organization Report No.
Performing Organization Name and Address Information Sciences and Human Factors Division NASA Office of Aeronautics and Space Technology Washington, D.C. 20546	10. Work Unit No. 11. Contract or Grant No.
Sponsoring Agency Name and Address National Aeronautics and Space Administration Washington, D.C. 20546	13. Type of Report and Period Covered Conference Publication 14. Sponsoring Agency Code

Supplementary Notes

Abstract

Progress reports and technical updates of programs being performed by NASA Centers are covered. Presentations in viewgraph form, along with abstracts, are included for topics in three categories: computer science, data systems, and space station applications. The Symposium was held at the Xerox Training Center, Leesburg, Virginia, from April 16 to 18, 1985. The Symposium schedule and a list of participants are included.

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17. Key Words (Suggested by Author(s))	18. Distribution Statement
Computer Science Data Systems Space Station	[redacted]

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of Pages	22. Price
Unclassified	Unclassified	398	

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Computer Science and Data Systems Technical Symposium

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Section 2: Data Systems Program (Cont.)

Section 3: Space Station Focused Technology

INTRODUCTION

The Computer Sciences and Data Systems Technical Symposium was held to respond to the communications challenges posed by the rapidly advancing technical arena surrounding NASA personnel. This was the second meeting in what will be periodic gatherings. The intended purpose of these meetings is to bring NASA people together to present their progress, to air their thinking and, in general, to discuss the nature and results of their work within the agency on a wholly technical level. These meetings are not intended as a forum for program reviews, budget presentations or advocacy hearings.

NASA personnel have long been recognized as prolific contributors to the journals of technical societies and organizations within the aerospace community. Symposiums such as this one, organized to improve the interchange of technical information and understanding within NASA, have resulted in valuable connections. These meetings will be continued. The Proceedings of the April 1985 Computer Sciences and Data Systems Technical Symposium are presented to provide a legacy for the latest gathering and a springboard to the next.

A VHSIC GENERAL PURPOSE PROCESSOR

H. F. BENZ
NASA LARC
APRIL 17, 1985

INTERNATIONAL TRAFFIC IN ARMS REGULATIONS

TITLE 22, CODE OF FEDERAL REGULATIONS PARTS 121-128

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BENEFITS TO NASA DATA SYSTEMS PROGRAM

THE VHSIC PROGRAM OFFERS NASA AND ITS CONTRACTORS ASSURED AVAILABILITY OF MIL-SPEC EMBEDDED COMPUTER COMPONENTS AND INTEGRATING CAD/CA~~E~~M AND SOFTWARE DEVELOPMENT SUPPORT TO GIVE LOW SYSTEM LIFE COSTS FOR DATA MANAGEMENT SYSTEM ON SPACE STATION AND EOS.

SUMMARY

THIS TALK WILL BRIEFLY REVIEW PROGRESS, TO DATE, BOTH IN THE DoD VHSIC PROGRAM AND IN THE NASA VHSIC RELATED INSERTION DEVELOPMENT OF A GENERAL PURPOSE PROCESSOR.

TOPICS:

LONG TERM OBJECTIVE OF LARC PROGRAM

RELATED PROGRAMS

APPROACH

RESULTS AND ACCOMPLISHMENTS

RELATIONSHIP TO NASA PROGRAMS

LONG TERM PLANS

SHORT TERM PLANS

SUMMARY

LONG TERM OBJECTIVES:

OAST PROGRAM:

TO CO-DEVELOP WITH THE DoD VHSIC PROGRAM A GENERAL PURPOSE HIGH DATA RATE SIGNAL PROCESSOR AND THE ACCOMPANYING HANDS ON TECHNOLOGY BASE INCLUDING CAD/CAM SYSTEM AND SOFTWARE DEVELOPMENT TOOLS SUITABLE FOR CORE SUBSYSTEM PROCESSING REQUIREMENTS.

SPACE STATION:

TO DELIVER VHSIC TECHNOLOGY TO THE SPACE STATION PROJECT AS A TECHNOLOGY FOR INSERTION INTO IOC; TO DEMONSTRATE READINESS BY A SET OF INTERLOCKING STUDIES WITH BRASSBOARD DEMONSTRATION; TO INSERT THIS TECHNOLOGY INTO SPACE STATION DATA MANAGEMENT SYSTEM TEST BED; TO USE THIS INSERTION TO LEARN HOW TO UPGRADE DMS TO FOC.

EOS:

TO DELIVER VHSIC TECHNOLOGY TO THE EOS COMMUNITY OF USERS AS A TECHNOLOGY FOR IMPLEMENTATION OF ONBOARD PROCESSING ELEMENTS FOR HIGH DATA RATE SENSORS.

IMPORTANCE OF PROBLEM

- NASA MUST ASSURE A HIGH RELIABILITY LONG LIFETIME COMPONENT TECHNOLOGY FOR ITS MISSIONS AND MUST HAVE A TECHNICALLY AGGRESSIVE POSTURE IN DEALING WITH ITS SYSTEMS CONTRACTORS.

- THE DoD RECOGNIZED THIS NEED IN 1979 AND IS CAPITALIZING THEIR WEAPONS SYSTEMS CONTRACTORS WITH THE TECHNOLOGIES OF SYSTEM INTEGRATION, IC DESIGN, FABRICATION, AND TEST TO MEET THEIR EMBEDDED SYSTEM NEEDS, AND ARE ALLOWING THEIR CONTRACTORS TO VERTICALLY INTEGRATE THEIR WEAPONS SYSTEMS DEVELOPMENTS.

- NASA SHOULD PARTICIPATE AND LEVERAGE AGAINST THE DoD TO ASSURE THAT ITS LONG TERM NEEDS ARE MET, SINCE NASA AND THE DoD SHARE CONTRACTORS ON MAJOR SYSTEMS BUILDS.

RELATED R&D

DoD VHSIC PROGRAM

- PHASE 1, HALF OF CONTRACTORS COMPLETE
  ALL CONTRACTORS IN FIELD ENHANCEMENT
- PHASE 2, THREE CONTRACTS AWARDED
  ALL ORGANIZING
  FIRST CHIP FROM EACH CONTRACTOR, COMMON BIU
- AF VHSIC 1750A GPC AT TRW/WESTINGHOUSE

NASA INSERTION ACTIVITIES

- WORK REPORTED HERE
- JPL MAX ARCHITECTURE
- AMES AI PROCESSOR

ENHANCED CAPABILITY OF EMBEDDED PROCESSING

- VHSIC SPEED AND POWER ENHANCEMENTS NECESSARY TO ACCOMMODATE INITIAL ADA INEFFICIENCIES
- LONG TERM DoD INVESTMENT/COMMITMENT
  - LONG TERM CONTINUING AVAILABILITY OF MIL-SPEC QUALIFIED COMPONENTS
- LOW SYSTEM LIFE/PROGRAMMING COSTS
  - BUILT IN TEST TO CHIP LEVEL TO FACILITATE MAINTAINABILITY
  - HARDWARE DESCRIPTIVE LANGUAGE TO FACILITATE HARDWARE FUNCTIONAL UPGRADABILITY
  - ADA LANGUAGE ACCOMMODATION
- POTENTIAL FOR SPACE QUALIFICATION

TECHNICAL APPROACH

- TO GENERATE VHSIC PROCESSOR SYSTEMS CONCEPTS EMBODYING DIRECTED GRAPHS AND PETRI NETS TO ALLOW QUASI STATIC REPARTITIONING OF HIERARCHICAL PROCESSOR TOPOLOGIES TO ACCOMMODATE HIGH PERFORMANCE DATA DRIVEN REQUIREMENTS IN THE SAME CONFIGURATION AS REDUNDANT, SELF-CHECKING, SELF-TESTABLE SYSTEM REQUIREMENTS.

- TO PROVE CONCEPTS IN LABORATORY ENVIRONMENT FOR USER FRIENDLY HARDWARE INSERTION/PLANNED SCARRING IN IOC AND FOC SPACE STATION SUBSYSTEMS.

- TO DETERMINE FEASIBILITY OF FLYING SUCH A SYSTEM TO EVALUATE SEU PERFORMANCE IN OPERATING ENVIRONMENT.

- TO INTEGRATE INTO TEST BEDS TO FACILITATE DMS SYSTEM INTEGRATION AND DEVELOPMENT OF SCARRING CONCEPTS.

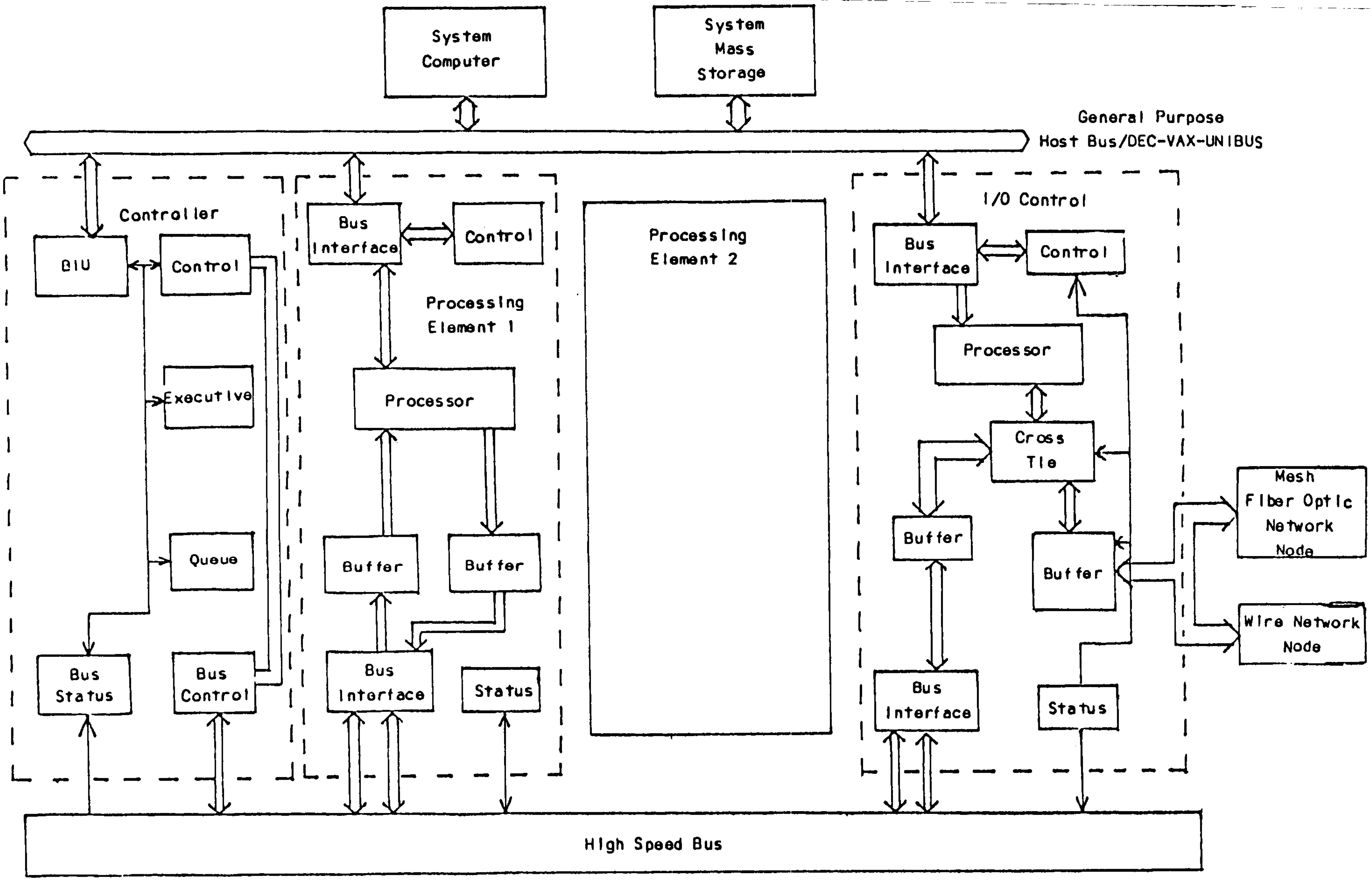


Fig. 1. High-Speed Processor

SUBSYSTEM TARGETS

HARDWARE

VHSIC SPACE STATION GP BRASSBOARD

- PARTITIONED SUBSYSTEM OF LARGER ARRAY
- 10 VHSIC CHIPS EXCLUSIVE OF MEMORY
- 3-5 MIPS DAIS
- 15-50 WATTS
- HIGH-SPEED INPUT/OUTPUT NODE
- INTEGRABLE INTO SPACE STATION DATA MANAGEMENT SYSTEM TEST BED

EXERCISER

- CONVENTIONAL MINICOMPUTER HOSTING COMPILERS, HARDWARE AND SOFTWARE DIAGNOSTICS, AND PROGRAM DEVELOPMENT TOOLS

SOFTWARE

- ADA (OR PASCAL) COMPILER RESIDENT ON MINICOMPUTER HOST
- EXECUTION OF SINGLE STRING PROGRAMS ON SUBSYSTEMS, INCLUDING CLASS II PROCESSING
- 1750A OR 1862 INSTRUCTION SET ARCHITECTURE WITH CONTROLLED USE OF XOP'S
- STAND ALONE OPERATION
- PROVISIONS FOR EXTENDED ARRAY SOFTWARE

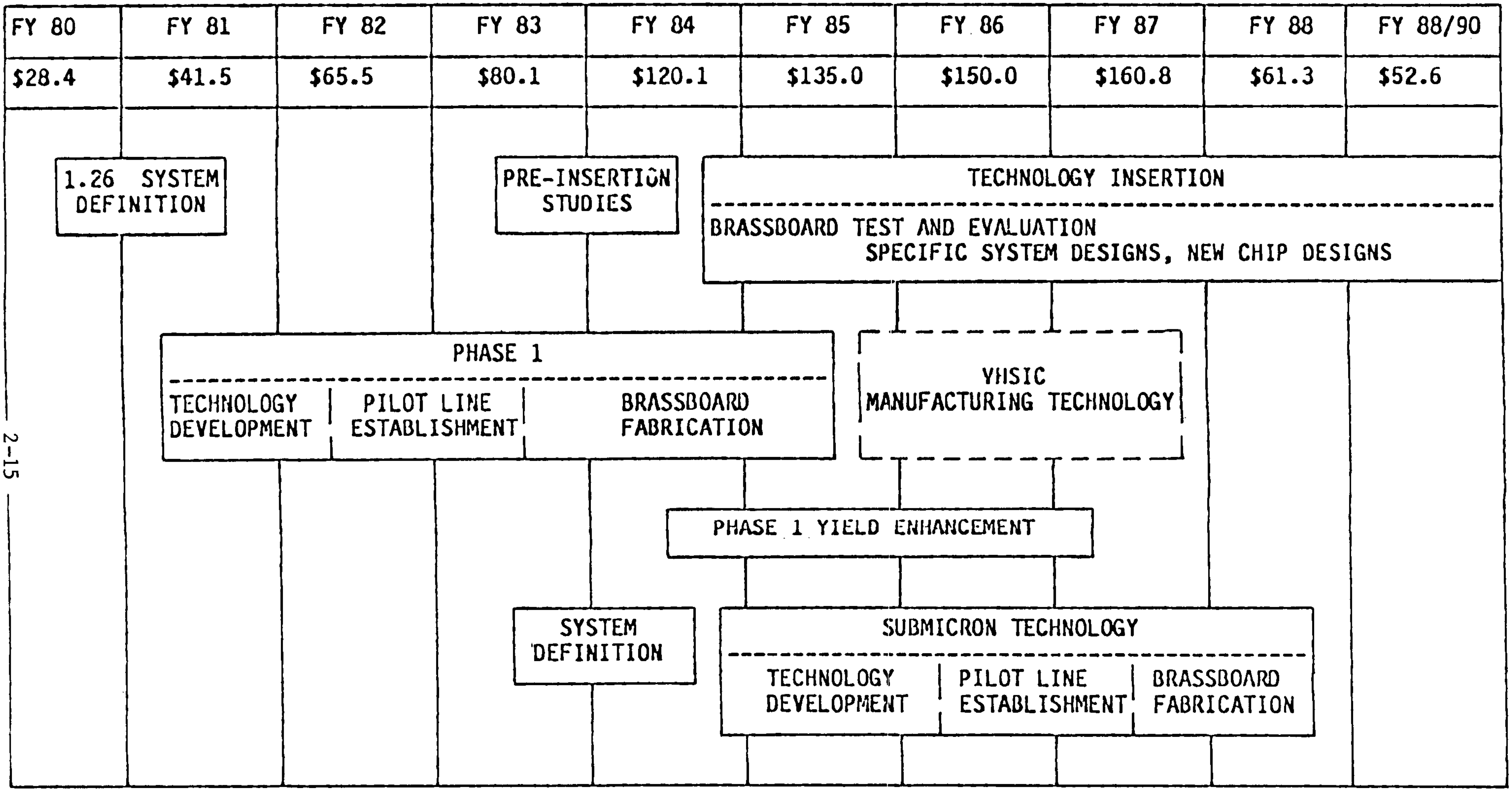
'85 ACCOMPLISHMENTS TO DATE

- FIRST LEVEL DGM TOOLS UP AND RUNNING ON IAS-VAX
  - NOT USER FRIENDLY
  - 2 GRAPH USERS TO WORKSHOP, 1 PROGRAMMER TO ADA SCHOOL
- PROCESSOR STUDY AT WESTINGHOUSE
  - INITIAL CONFIGURATION
  - CONCEPT FOR ASYNCHRONOUS TRIPLEX TASK DISPATCHMENT
  - OPERATING SYSTEM MODELING
  - CONCEPTS EMBODIED IN AF 1750A AWARD TO TRW/WESTINGHOUSE
- EOS INSERTION STUDY
  - 100^+ INSTRUMENTS SURVEYED
  - 24 INSERTION CANDIDATES IDENTIFIED AND MAPPED TO BRASSBOARDS
  - DRAFT REPORT IN APPROVAL CYCLE
  - 3 INTERCENTER BRIEFINGS GIVEN
- BACK UP PROCESSOR FROM TI CONTRACTED WITH ARMY
- BACK UP CONFIGURATION MODELING CONTRACTED WITH RTI, ADAS-TI
- VHSIC WORKSHOP AT JSC IN NOVEMBER
- LARC DECISION TO IMS INVESTMENT IN CAD/CAM
- VHSIC COMPATIBLE HW TO FACILITATE "HANDS ON" IN PROCUREMENT
- FLIGHT EXPERIMENT IDENTIFIED FOR DATA SYSTEM TO SS-TDAG
- SELF-TESTABLE 1750A DESIGN SBIR PROGRAM COMPLETED PHASE I, PHASE II AWARDED

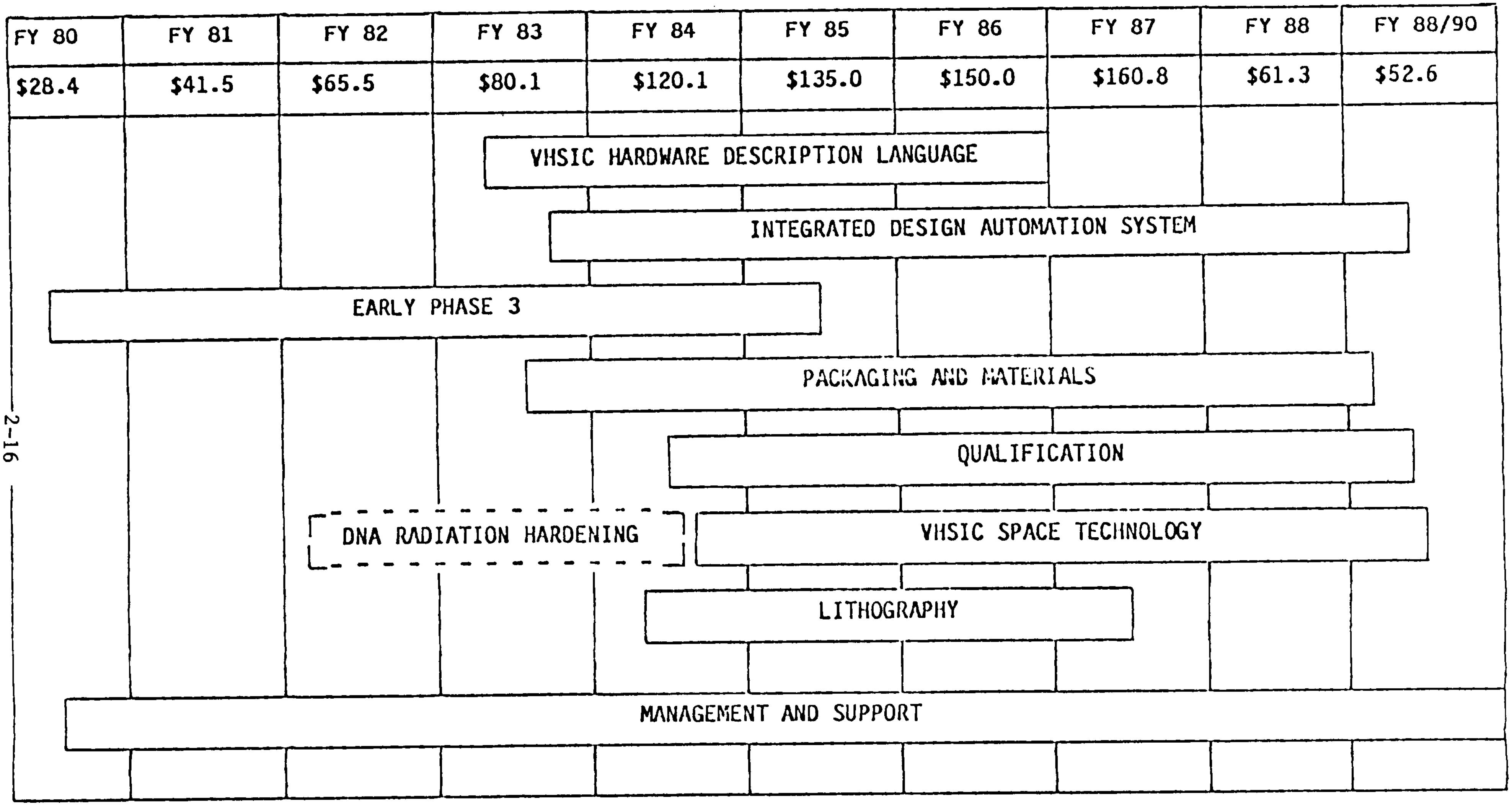
EXPECTED DURING BALANCE OF '85

- COMPLETION OF WESTINGHOUSE AND NICHOLS STUDIES
  - SIMULATION OF 4 PROCESSOR CONTROLLER CONFIGURATION
  - PROJECTION OF IMPLEMENTATION COSTS FOR FULL UP SYSTEM
  - INITIATION OF OPERATING SYSTEM FOR M OF N FAULT DETECTION
- FIRST VHSIC COMPATIBLE HARDWARE IN-HOUSE AND OPERATING (FAIRCHILD 9450 CHIPSET IN AVIONICS BRASSBOARD)
- ADVOCACY AND PLAN FOR RAD TOLERANT EOS PROCESSOR DEVELOPMENT
- DEFINED ROLE IN VHSIC 1750A SPACE TECHNOLOGY PROGRAM

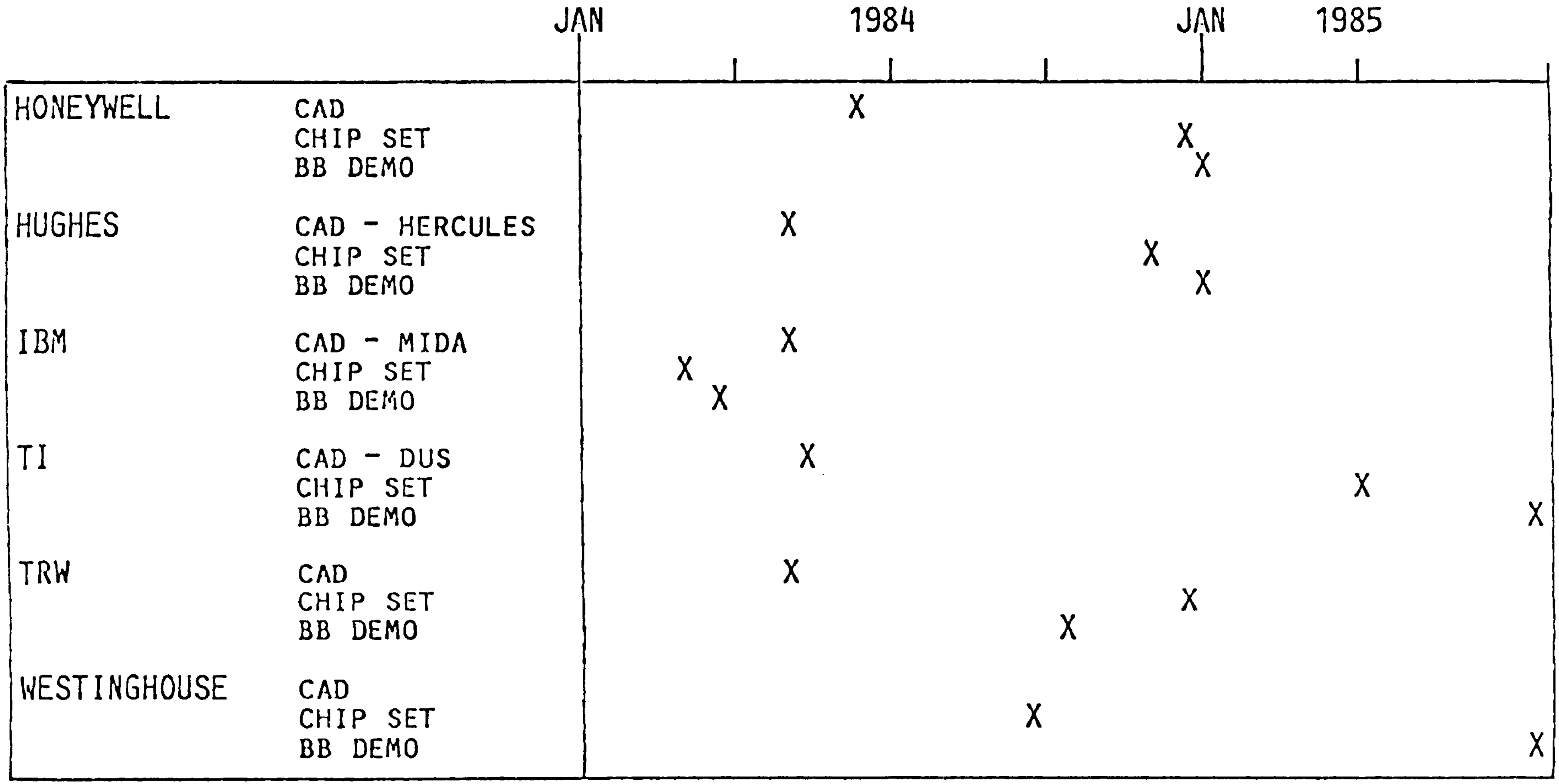
VHSIC PROGRAM ROAD MAP

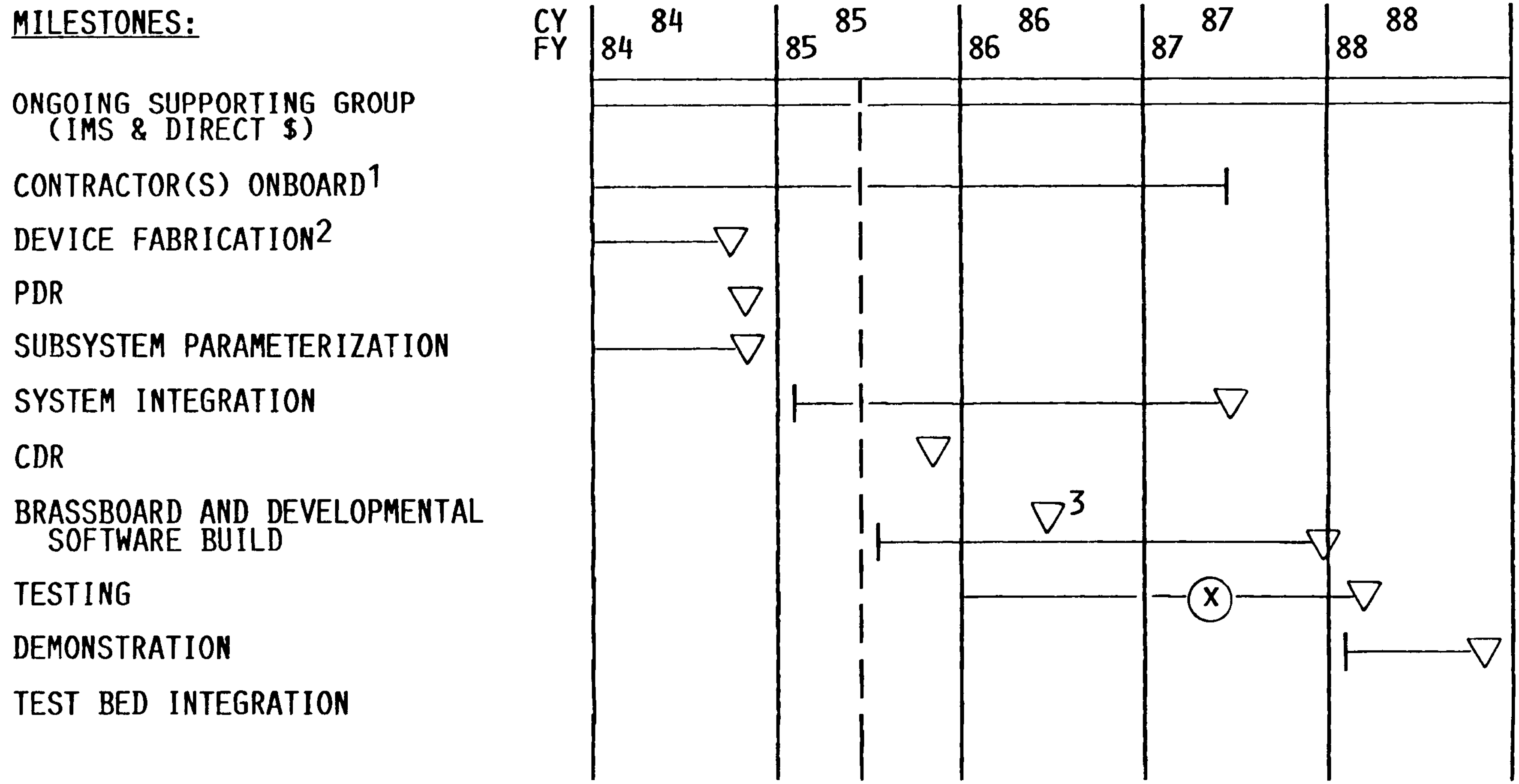


VHSIC PROGRAM ROAD MAP
(CONTINUED)



MAJOR MILESTONES FOR PHASE I





[1] ASSUMING NASA/DOD MOU ACTIVITY
[2] AS PART OF ONGOING DOD PROGRAM
[3] TECHNOLOGY IS FROZEN HERE
[4] STUDY RESULTS AVAILABLE JULY 84, IN DRAFT FORM
(X) INTERIM TEST DATA AVAILABLE

RESOURCES: FY	83	84	85	86	87	88
R&D	200	400 (180)	560 (100)	2000	2000	2000
MP	2	3	5	10	10	10

LONG TERM PLANS

COMPLETE AND INSERT PROCESSOR SUBSYSTEM INTO SS DMS TEST BED BY C/D PDR

DEVELOP POTENTIAL SCARRING METHODS FOR BOTH HARDWARE AND SOFTWARE BY C/D PDR

EXAMINE FEASIBILITY OF SCARRING HARDWARE THROUGH POTENTIAL FOC TEST BED BY C/D CDR

EXAMINE POTENTIAL OF DEVELOPMENT OF VHSIC SPACE PROCESSOR WITH DoD AND EOS FOR IMPLEMENTATION IN 1990'S

PLAN FOR VHSIC II UPGRADES INTO NASA SYSTEMS BY MID 90'S

SUMMARY

- REVIEW PROGRESS
- PROGRESS INDICATES SUCCESS

JPL

MAX

A SPACE STATION COMPUTER OPTION

D.B.Smith
R.D.Rasmussen

P-12

JPL

General Purpose Space Computing

- Typified by most
  - engineering subsystems
  - payloads
  - other "intelligent" devices

- Specifically excludes
  - top end, special-purpose signal processors
  - low end, in-circuit µ-processor applications

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CHARACTERIZED BY

- Embedded, real-time applications
- Both synchronous, cyclic operation and asynchronous, event driven operation
- Both computationally intensive (e.g. signal processing, guidance) and data intensive (e.g. command and telemetry) processing
- Wide range of throughput and memory requirements
- Range of fault tolerance requirements from none to full, uninterruptable operation through faults or damage
- Maintainability, including capability for on-line substitution in critical systems

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MAX HARDWARE FEATURES

- General purpose computer module
  - Small, light weight, & low power
  - Radiation hard & single event upset immune
  - ≈ 1 Million Whetstone equivalent instructions per second (floating point)
  - 256 Kbytes (expandable) memory
  - High speed communication ports & memory mapped I/O
  - Global semaphore capability without shared memory

- Special features support
  - Multi-computer concurrency
  - Software implemented fault tolerance
  - Spatial distribution for damage tolerance

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MAX SOFTWARE FEATURES

- Conventional programming and test environments
- Layered software design supporting
  - high level languages
  - real time, multi-tasking & task migration
  - packet communication
  - data management
  - concurrency
  - fault tolerance
- Optional low resolution data-flow concurrency support

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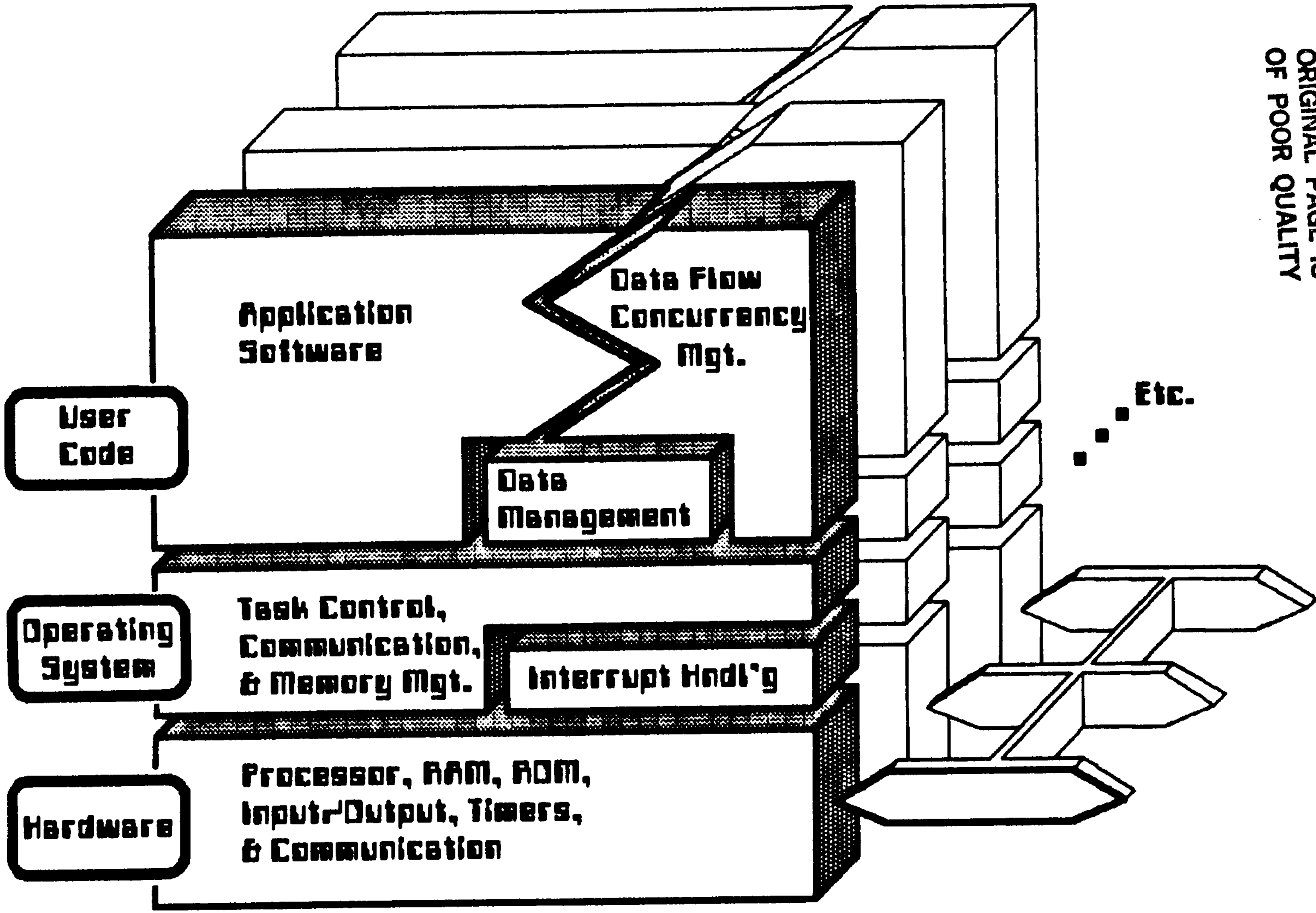
MAX LAYERED ARCHITECTURE



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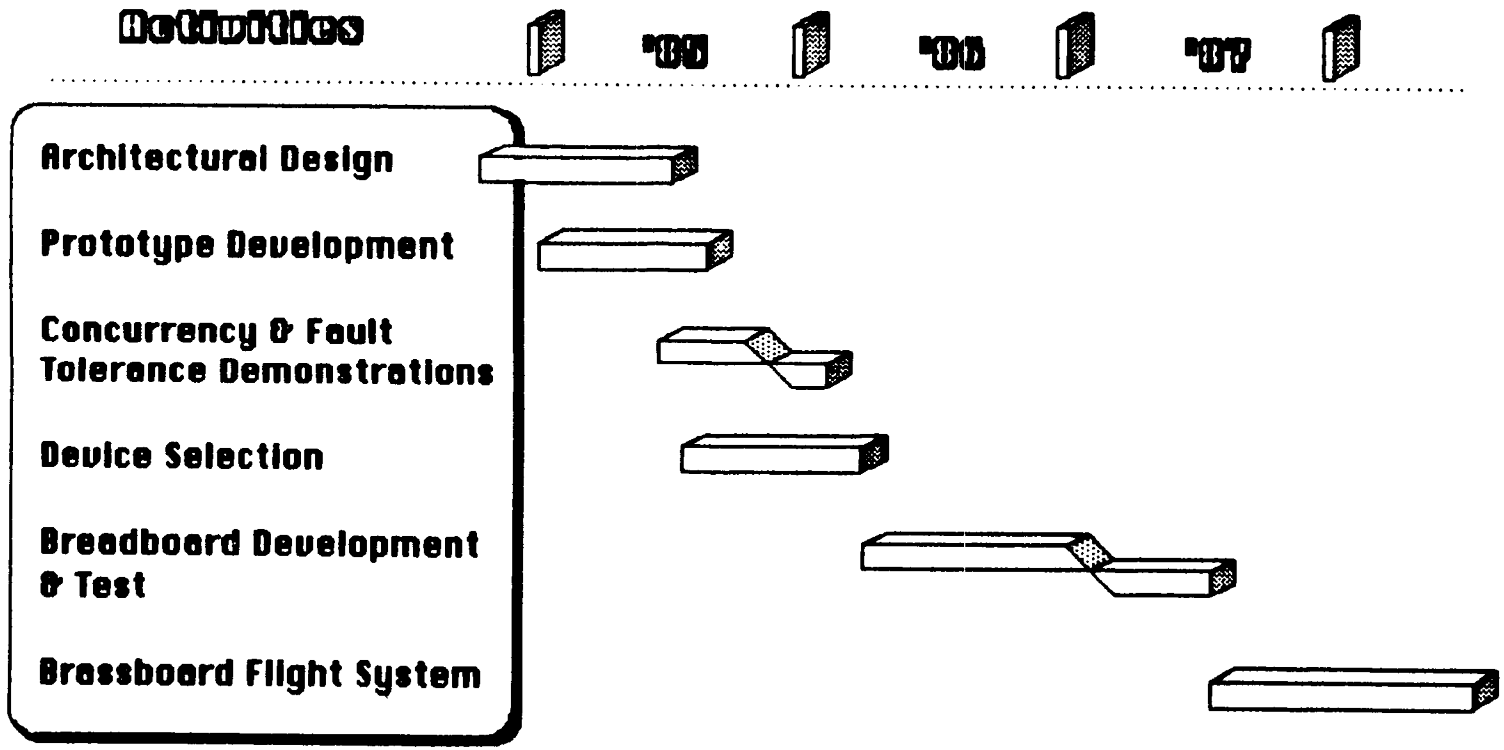
MAX DEVELOPMENT PLAN



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IMPLEMENTATION OPTIONS

- Low power bipolar devices are susceptible to single event upset
- Preferred device technology is CMOS
  - High density CMOS is fast, but low power
  - Can be made single event upset immune
- Existing CMOS part sets include
  - EPIC bit-slice family & related parts
  - 2900 family bit-slice component emulations
  - Custom standard cell and gate array components
  - 8085, 80C86 and 1802 μ-processors (& selected peripheral parts)
  - Memory components
- Comparable VHSIC components in development

JPL

PROMISING NEW ARRIVAL

- 2 micron (10-15 MHz) CMOS emulation of National Series 32000™ and supporting devices by Sandia National Laboratories
  - 32032 and 32016 μ-processors
  - 32081 Floating Foint Unit
  - 32201 Timing Control Unit
  - 32202 Interrupt Control Unit (plus timers & I/O)
  - 8K×8 static RAM, 32K×8 ROM, 32K×8 EEPROM, & non-volitile RAM
  - 1K (and 2.5K -10K ?) gate array
  - Standard cells (up to 30,000 transisters per chip)
  - Miscellaneous glue chips (buffer, latch, decoder, byte I/O,...)
  - Bus arbiter & DMA controller under consideration
- Replacement compatible with commercial versions

ADVANTAGES

- Prototyping can begin now with commercial parts
- Throughput comparable to VAX-11/750 (≈ 1 MIPS)
- Modern architecture explicitly and efficiently supporting
  - modular programming
  - complex data structures
  - structured language control flow, etc...

  Result» lower cost, more compact, more reliable code

- Small chip count and small physical size
- Clean support for custom slave processors
- Wide range of commercially available support tools
- Potential direct path to subsequent VHSIC level integration (NSC is a VHSIC phase I subcontractor to WEC)

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Radiation Hardness

- Total dose hardness of 1×10^{6} Rads (Si)
- No upset to 1×10^{9} Rads (Si) /sec
- No upset from 140 MeV Krypton, any angle

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SANDIA DEVELOPMENT PLAN

- NSC enthusiastic and involved in program (contract not yet signed as of March 85)
- Engineering samples of 32016 and all other components (except 32032) available by fourth quarter of 1988
- 32032 available by second quarter 1989
- Six months from engineering samples to production quantities
- JPL considering test & qualification of commercial parts (both NSC & second source TI) for acceptibility in low dose environments

N87-29147

ONBOARD HIGH DATA RATE SIGNAL PROCESSING AND STORAGE

WARNER H. MILLER
NASA/GSFC
4/17/85

HISTORY

THE NEED TO INCREASE THE INFORMATION RETURN FROM SPACE-BORNE IMAGING SYSTEMS HAS GROWN DRAMATICALLY DURING THE PAST DECADE. THE GROWTH IN THE USE OF MULTISPECTRAL DATA HAS RESULTED IN THE NEED FOR GREATER SPATIAL RESOLUTION AND SPECTRAL COVERAGE. INCREASES IN RESOLUTION, FIELD OF VIEW AND NUMBER OF SPECTRAL BANDS HAVE ALL POINTED IN THE SAME DIRECTION...TOWARD INCREASED DATA RATES AND HIGHER BANDWIDTH REQUIREMENTS. FURTHERMORE, THE DATA RATE IMPLIED BY THESE IMPROVED PERFORMANCE CHARACTERISTICS CAN BE EXPECTED TO GROW MORE RAPIDLY THAN SPACECRAFT TELECOMMUNICATIONS CAPABILITIES. ALTHOUGH THE TELECOMMUNICATIONS CAPABILITY PLANNED THROUGH THE 1980S IS RELATIVELY LARGE, FEASIBILITY STUDIES ON SOLID STATE MULTISPECTRAL IMAGING INSTRUMENTS IN SUPPORT OF LAND OBSERVING SYSTEMS, USING CHARGE COUPLED DEVICES (CCD) TECHNOLOGY, UNCOVER DATA RATES THAT EXCEED THE TELECOMMUNICATIONS CHANNEL CAPACITY. ONBOARD SIGNAL/DATA PROCESSING WILL PLAY A PIVOTAL ROLE IN SATISFYING THE NEED FOR MORE INFORMATION BY UTILIZING THE AVAILABLE COMMUNICATION CHANNEL AT HIGHER EFFICIENCY.

THE OBJECTIVE OF THIS PROGRAM IS TO ADVANCE THE STATE-OF-THE-ART IN ONBOARD IMAGE DATA PROCESSING AND STORAGE THROUGH THE USE OF ADVANCE GAAS INTEGRATED CIRCUIT TECHNOLOGY. AS GAAS INTEGRATED CIRCUIT TECHNOLOGY MATURES, IT WILL BE ADVANTAGEOUS FOR SMART SENSOR SIGNAL PROCESSING, WHERE THE HARDWARE REQUIREMENT IS HIGH DATA RATE PROCESSING, AT LOW POWER AND INCLUDING RADIATION TOLERANCE.

FUTURE PLANS

THE OBJECTIVE OF AN EXISTING CONTRACT WITH ROCKWELL INTERNATIONAL IS TO MANUFACTURE A MICROPROCESSOR CHIP SET USING GAAS. THIS CHIP SET, WHEN FUNCTIONING TOGETHER ON A SINGLE CIRCUIT BOARD, WILL PERFORM HIGH DATA RATE IMAGE PROCESSING ALGORITHMS. THE INITIAL CHIP SET WOULD CONSIST OF FOUR DEVICE TYPES WITH THE ABILITY TO ADD FAMILY PARTS AS FUTURE SYSTEM DEMANDS REQUIRE. THE DEVICE TYPES WOULD INCLUDE: CONTROL SEQUENCER WITH ROM, 8 BIT SLICE GENERAL PROCESSOR, I/O AND INTERRUPT CONTROLLER, AND A GENERAL PURPOSE RAM. THIS CHIP SET USING GAAS TECHNOLOGY WOULD PRODUCE A FUNCTIONAL COMPUTER SYSTEM OPERATING WITH A 5 NANOSECOND MICROCYCLE TIME. IN 1985, THE CHIP SET ARCHITECTURE WILL BE DEFINED, AND THE CHIP

SET CRITICAL SPEED PATH ANALYZED TO ATTAIN A SYSTEM CLOCK RATE OF NO LESS THAN 200 MHZ. FOLLOWING TASKS WILL INCLUDE CHIP SET DESIGN, LAYOUT AND FABRICATION. FINALLY, THE CHIP SET WILL BE INTEGRATED ONTO A SINGLE CIRCUIT BOARD WITH THE CONTROL SEQUENCER, ROM MASK PROGRAMMED TO PERFORM AN IMAGING PROCESSING FUNCTION. WHEN CONFIGURING TWO 8-BIT SLICES OF THE GENERAL PROCESSOR, THE CHIP SET ARCHITECTURE WILL DEMONSTRATE EMULATION OF MIL-STD-1750A INSTRUCTION SET.

506-58-16

ONBOARD HIGH DATA RATE SIGNAL PROCESSING AND STORAGE

I. TECHNICAL OBJECTIVES

ADVANCE THE STATE-OF-THE-ART IN ONBOARD IMAGE SIGNAL PROCESSING AND STORAGE THROUGH THE USE OF ADVANCED GALLIUM ARSENIDE (GaAs) INTEGRATED CIRCUIT TECHNOLOGY.

II. TECHNICAL APPROACH

DESIGN, DEVELOP AND FABRICATE AN 8-BIT SLICE GaAs GENERAL PROCESSOR CHIP SET CAPABLE OF PERFORMING HIGH DATA RATE IMAGE PROCESSING ALGORITHMS. THE BIT SLICES CAN BE CASCADED TO PROVIDE DATA BUS WIDTH OF 8 BIT MULTIPLES (8, 16, 24, 32, 40). WHEN CONFIGURING TWO 8 BIT SLICES, THE CHIP SET ARCHITECTURE WILL DEMONSTRATE EMULATION OF MIL-STD-1750A INSTRUCTION SET.

WARNER MILLER
4/17/85

REAL TIME PROCESSING OF IMAGING ARRAYS

RELATIONSHIP BETWEEN SPATIAL RESOLUTION AND DATA RATE FOR ONE SPECTRAL BAND

ASSUMING 185K FOV AND AN EARTH VIEWING ALTITUDE OF 700KM

	IFOV (M)	# DET. PER FOV	INTEG. TIME (DWELL) (MSEC.)	PIXEL RATE	PIXEL PERIOD (MICRO SEC.)	SERIAL DATA RATE PER SPECTRAL BAND (B/SEC.)
	120	1542	17.7	87 KPPS	11.5	695.7 K
MSS	80	2313	11.8	196K	5.1	1.57M
	60	3083	8.9	347.7K	2.9	2.78M
	40	4625	5.9	782.4K	1.3	6.26M
TM	30	6167	4.4	1.39 MPPS	0.72	11.13M
	20	9250	2.9	3.13M	0.32	25.0 M
	15	12334	2.2	5.56M	0.179	44.5 M
ALOS/MLA	10	18500	1.47	12.5M	0.080	100.0 M

NASA RELATED R&D EFFORTS

* LASER COMMUNICATION (506-58-26)
  - CLOCK RECOVERY CIRCUITRY
  - MATCH FILTER
  - DATA DETECTOR AND MODULATOR

* RESEARCH OPTICAL SENSOR (666-51-70)
  - PIXEL AVERAGING
  - OFFSET SUBTRACTION
  - GAIN CORRECTION

* 150 MB/S REED-SOLOMON ENCODER/DECODER (310-20-46)
  - MULTIPLEXER/DEMULTIPLEXER

* COMPUTER VISION (488-32-02)
  - OFFSET SUBTRACTION/GAIN CORRECTION
  - SUN SHADE CORRECTION
  - CONTRAST ENHANCEMENT

WHY GaAs INTEGRATED CIRCUITS?

HIGH SPEED	100-200 PSEC GATE DELAYS
LOW POWER	0.5-2 MWATTS/GATE
RADIATION HARD	50 MRADS TOTAL DOSE
WIDE TEMPERATURE RANGE	-200°C TO 200°C

Rockwell International

ADAPTIVE PROGRAMMABLE PROCESSOR CHIP SET

8-BIT SLICE GENERAL PROCESSOR UNIT

CONTROL SEQUENCER AND ROM

GENERAL PURPOSE ROM/RAM

I/O AND INTERRUPT CONTROLLER

GATE ARRAY

Rockwell International

PERFORMANCE GOALS
ADAPTIVE PROGRAMMABLE PROCESSOR

CLOCK RATE:	200 MILLION CLOCKS PER SECOND
ADD TIME:	5 nsecs
8 x 8 MULTIPLY TIME:	25 nsecs

\- - - - - - - - - -

THROUGHPUT (PERFORMING NON-UNIFORM QUANTIZER): 150 MIPS

Rockwell International

PROGRAM HARDWARE DELIVERABLES

* THREE ADAPTIVE PROGRAMMABLE PROCESSING BOARDS

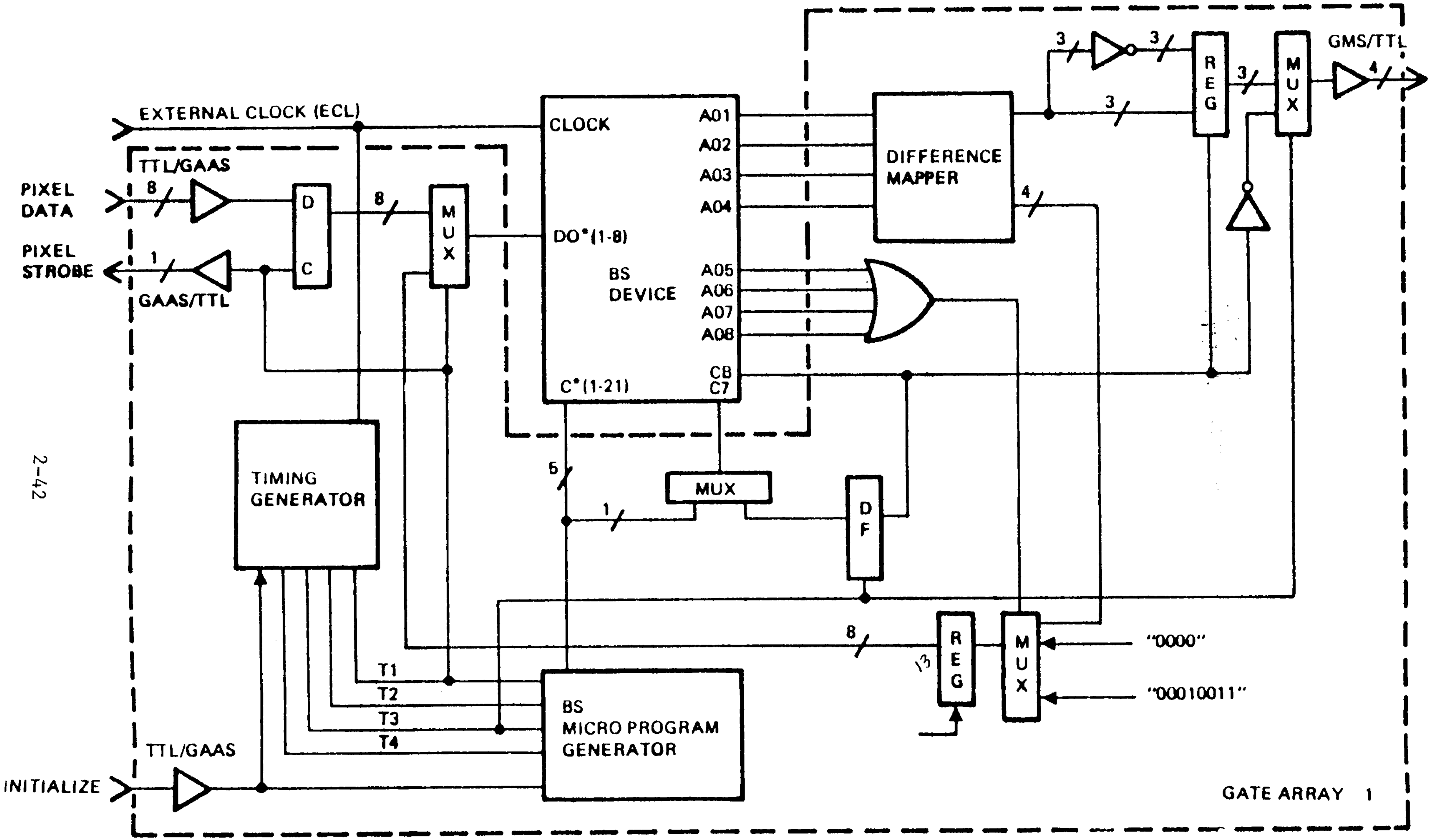
  ONE BOARD CONTAINING GATE ARRAY #1 AND ONE 8 BIT SLICE GENERAL PROCESSOR WHICH WILL PERFORM AN IMAGE DATA COMPRESSION ALGORITHM

  TWO BOARDS EACH WILL CONTAIN:
  - TWO 8 BIT SLICE GENERAL PROCESSORS
  - ONE CONTROL SEQUENCER WITH AN INTERAL ROM (32K)
  - TWO GENERAL RAM (128x8)
  - TWO GATE ARRAYS FOR I/O AND INTERRUPT CONTROLLER

  AND CONFIGURED TO EMULATE THE 1750A INSTRUCTION SET.

* SOFTWARE FOR THE FOLLOWING SIGNAL PROCESSING ALGORITHMS

  DPCM NOW UNIFORM QUANTIZER
  RADIOMETRIC CORRECTION
  DIGITAL FILTER
  (ONE TO BE DETERMINED).



The Non-Linear Quantrer Block Diagram

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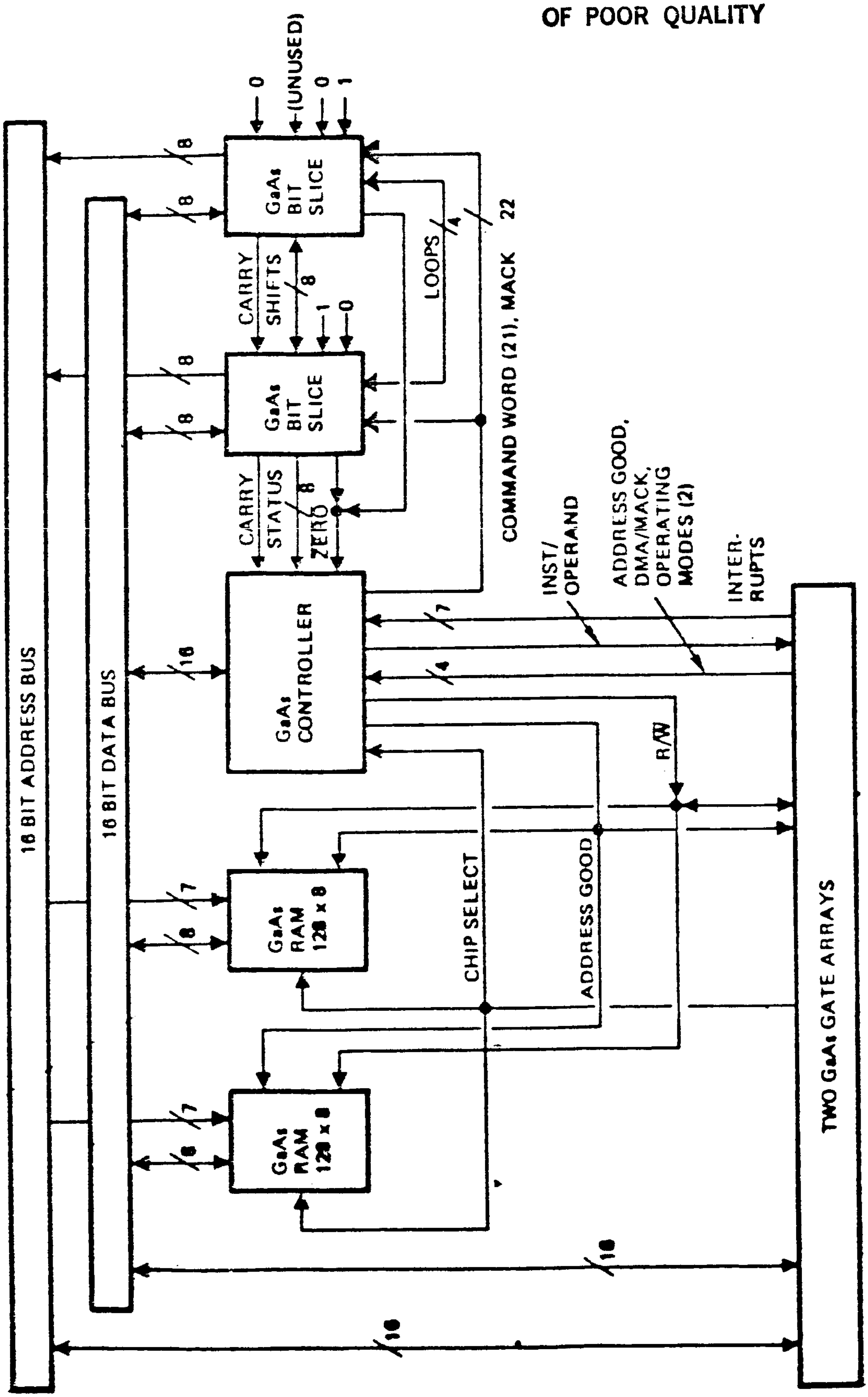
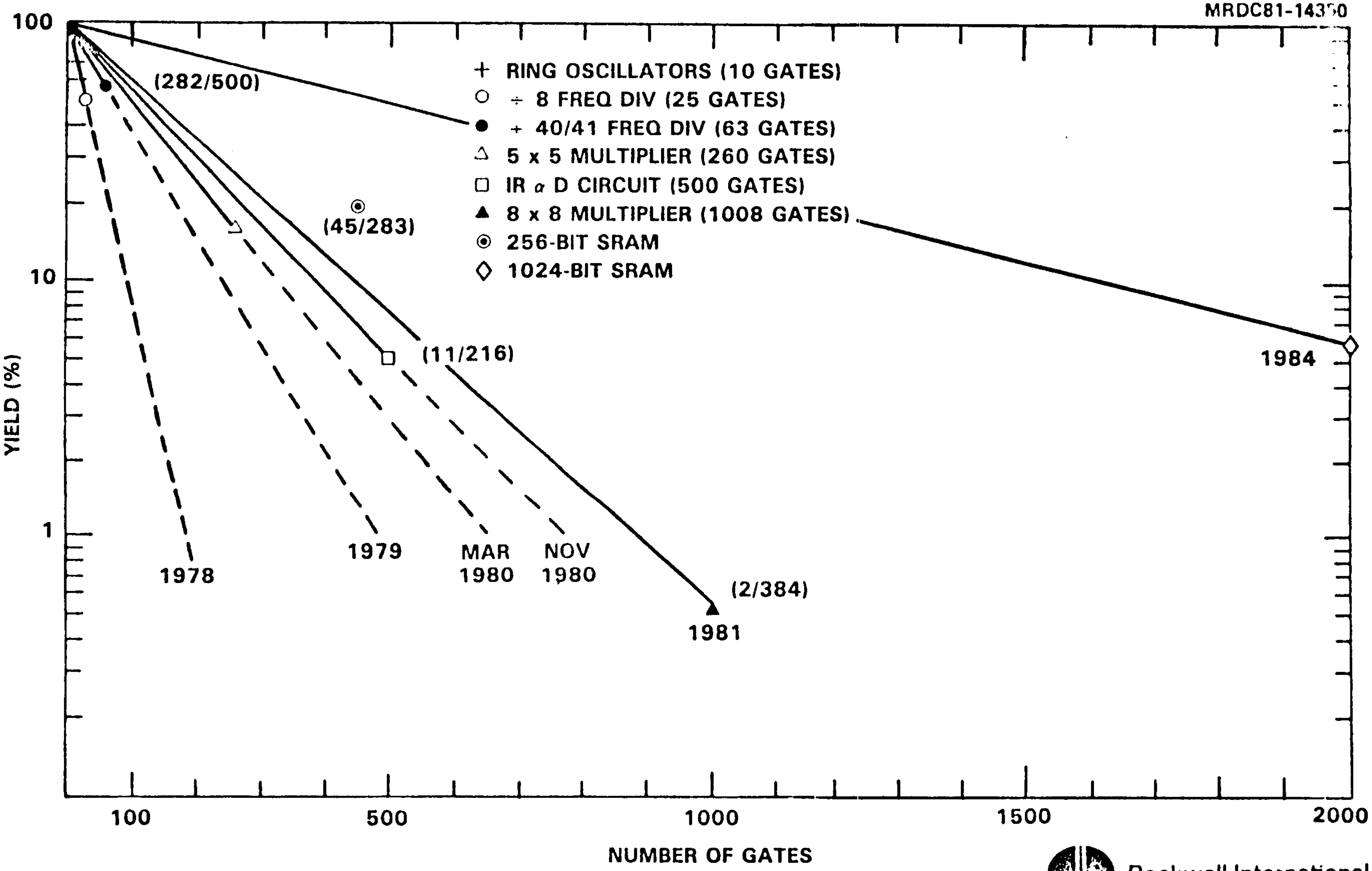


DESIGN CHARACTERISTICS

COMPLEXITY	
8 BIT GENERAL PROCESSOR	950 GATES
GATE ARRAY	437 GATES
CONTROLLER LOGIC	191 GATES
CONTROLLER MICROPROGRAM ROM	744x44 BITS
POWER PER DEVICE	5 WATTS

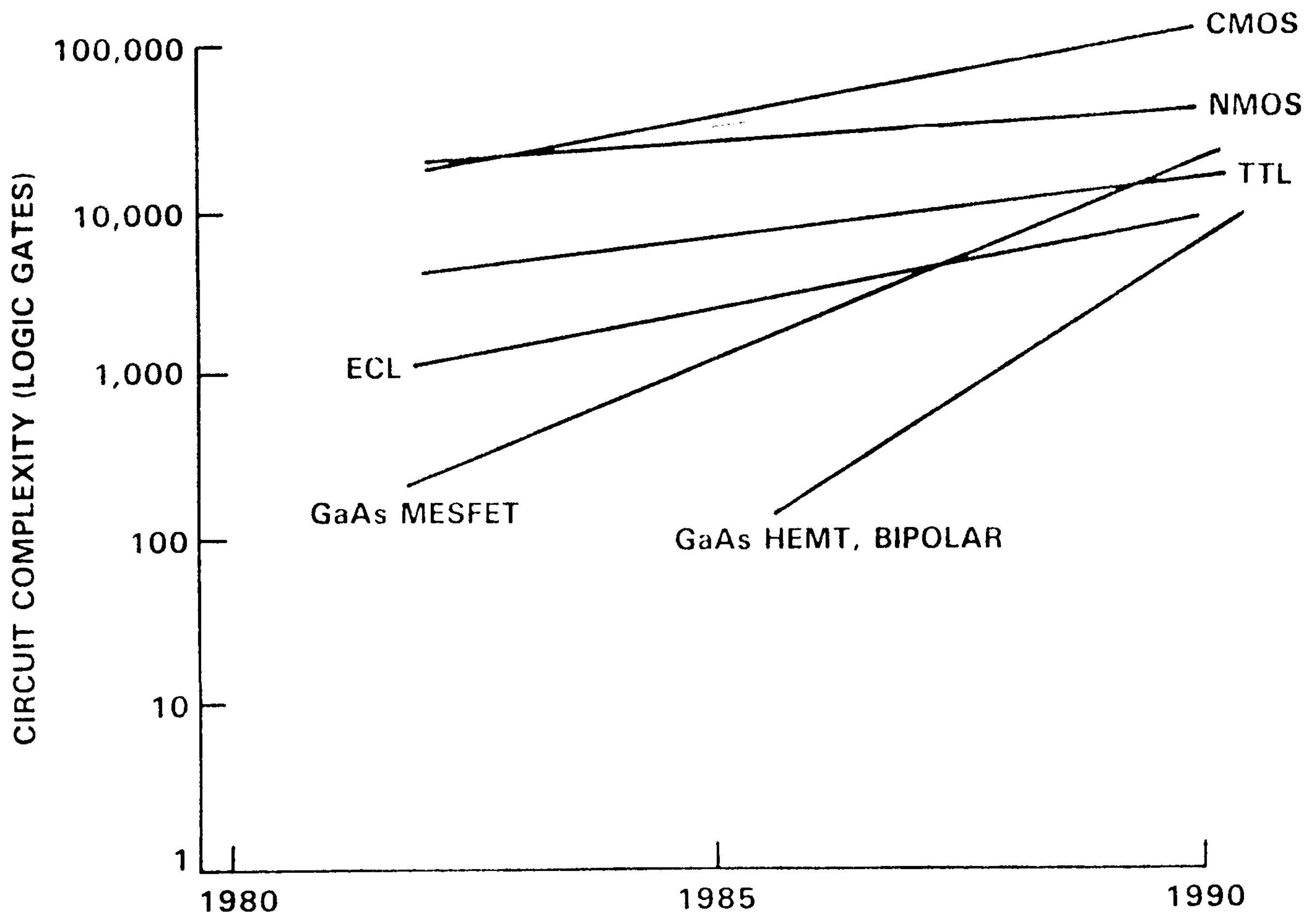
	8 BIT SLICE (2)	8 BIT SLICE (6)
EXECUTE TIMES		
16 BIT ADD (AIM)	3 CYCLES	3 CYCLES
16 BIT MULTIPLY (MIM)	11	11
32 BIT FLOATING PT. ADD (FAR)	46	5
1750A DIAS INSTRUCTION MIX (5 NSEC CYCLE PERIOD)	12 MIPS	27 MIPS

GaAs IC YIELD vs GATE COMPLEXITY



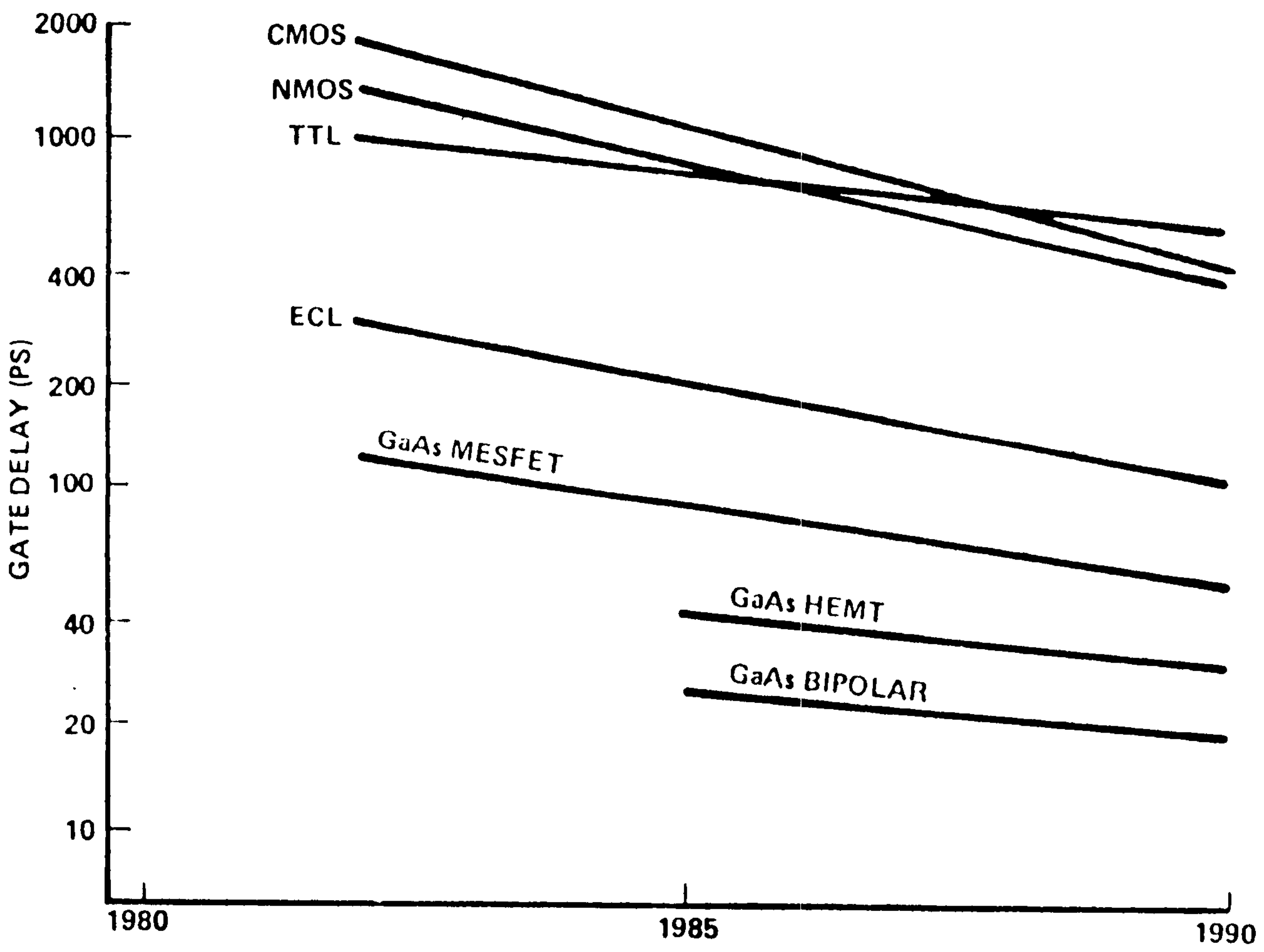
Rockwell International

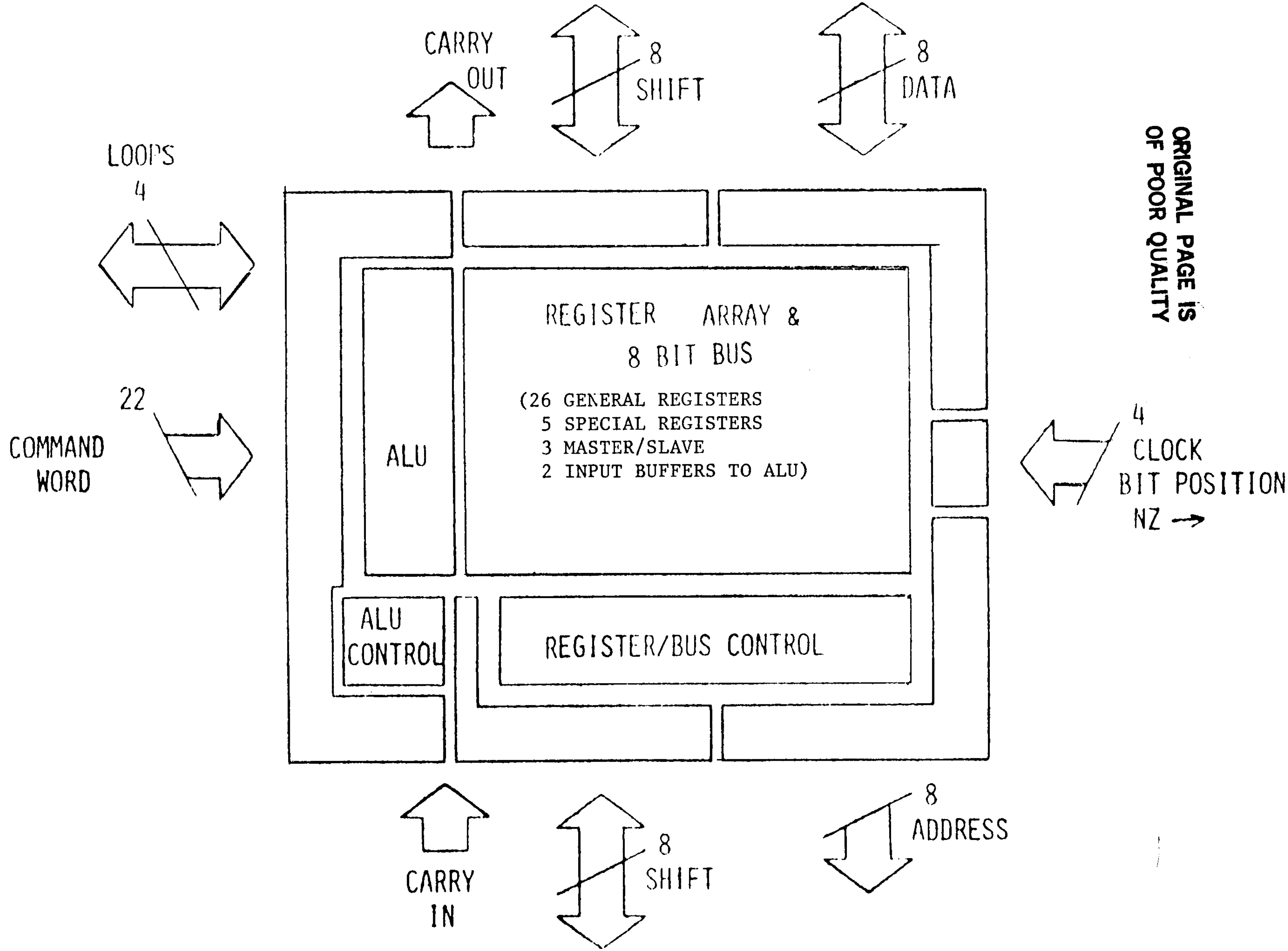
DENSITY COMPARISON OF SILICON AND GaAs INTEGRATED CIRCUITS



Rockwell International

SPEED COMPARISON OF SILICON AND GaAs DEVICES



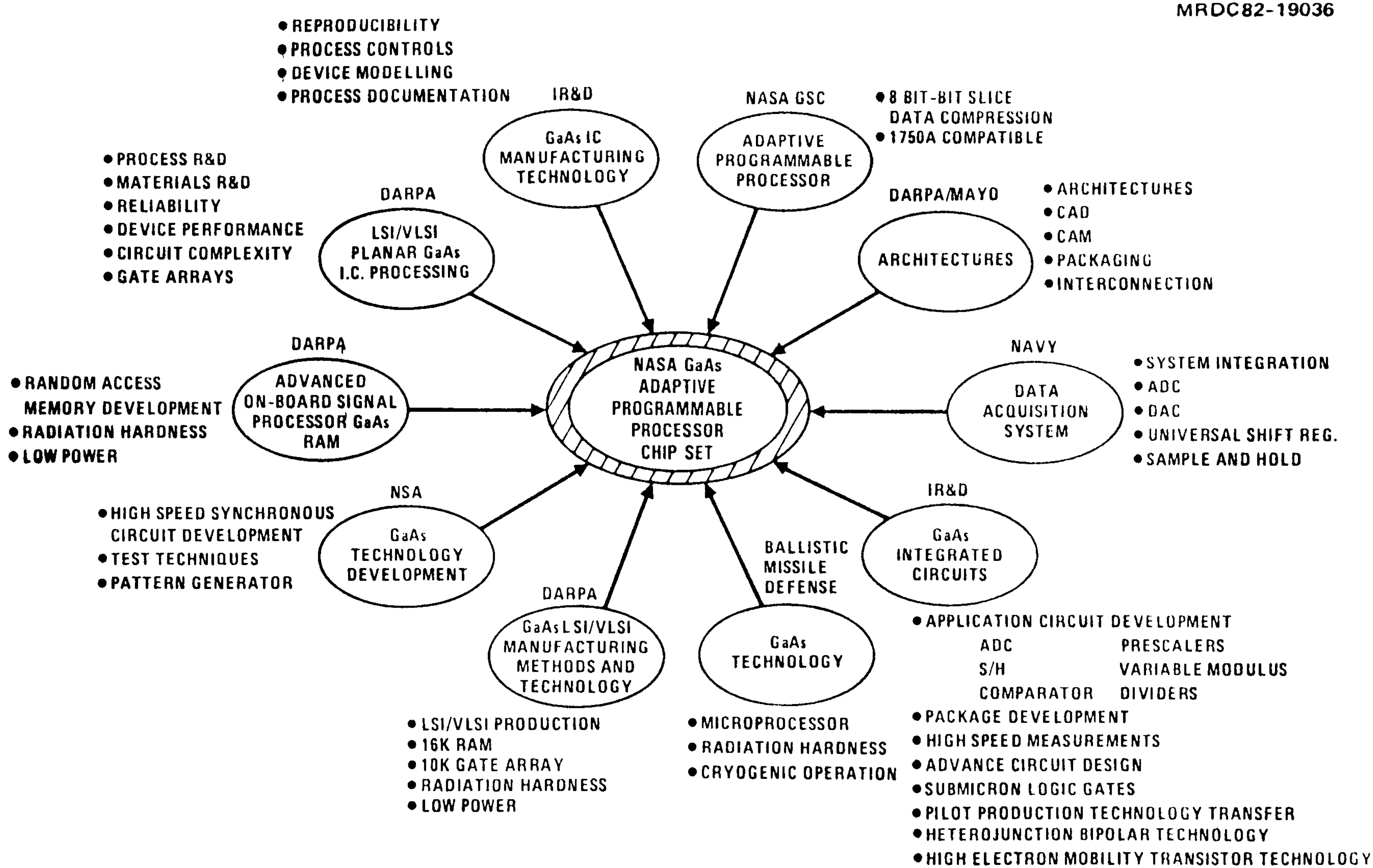


NASA 8-BIT SLICE BLOCK DIAGRAM

ACCOMPLISHMENTS FY84	
CONTRACT AWARD FOR GaAs APP CHIP SET	2/84
CHIP SET ARCHITECTURE	11/84
PLANNED ACCOMPLISHMENTS FY85	
BIT SLICE/DESIGN PDR (COMPLETED)	2/85
BIT SLICE/GATE ARRAY #1 CDR	6/85
FAB. BIT SLICE/GATE ARRAY	12/85
PLANS	
CONTROLLER/GATE ARRAY 2&3 FAB.	8/86
CHIP SET CIRCUIT TESTING	10/86
CIRCUIT BOARD FAB.	4/87
APP CHIP SET SYSTEM TEST	2/88
APP CHIP SET/HEMT TECHNOLOGY	6/89
SELECTED INSTRUCTION SET PROCESSOR (SISP)	2/90

ROCKWELL'S GaAs DIGITAL IC R&D PROGRAMS

MRDC82-19036



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Rockwell International

JPL

FLIGHT ARRAY PROCESSOR

I. INTRODUCTION

II. SPACEFLIGHT APPLICATIONS FOR ARRAY PROCESSORS

III. DESIGN CONSIDERATIONS FOR FLIGHT ARRAY PROCESSORS

IV. ISSUES REGARDING SPACEFLIGHT APPLICATIONS OF ARRAY PROCESSORS

N87-29148

WJR-4/17/85

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INTRODUCTION

- OBJECTIVES
  - DEVELOP AN ADVANCED HIGH SPEED ARRAY PROCESSOR FOR SPACE STATION USE.
  - MAKE SCIENTIFIC AND ENGINEERING INFORMATION AVAILABLE IN REAL TIME (OR FOR LATER USE).
  - ENABLE MORE EFFECTIVE USE OF DOWNLINK AND INTERSPACECRAFT COMMUNICATIONS, E.G., DATA COMPRESSION AND ENCODING.
  - MAKE DATA AND SIGNAL PROCESSING SOFTWARE EASIER TO DESIGN AND CODE AS WELL AS MORE RELIABLE.

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SPACEFLIGHT APPLICATIONS FOR ARRAY PROCESSORS

- APPROACH
  - USE AS BASELINE, TWO EXISTING PROGRAMS: NSCAT AND ADSP.
    - NSCAT - NASA SCATTEROMETER. FLOWN AS PART OF NAVY REMOTE OCEAN SENSING SYSTEM (NROSS). MEASURE OCEAN SURFACE WINDS.
    - ADSP - ADVANCED DIGITAL SAR PROCESSOR. GROUND-BASED EQUIPMENT BEING DEVELOPED BY JPL FOR PROCESSING SPACECRAFT EARTH OBSERVATIONS.

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DESIGN CONSIDERATIONS FOR FLIGHT ARRAY PROCESSORS

- NSCAT (FIGURE 1) - STUDY CONTRACT WITH STANFORD UNIVERSITY.
  - WIND MEASUREMENT RADAR (SCATTEROMETER);
  - ESTIMATE SURFACE WIND VELOCITY OVER OCEAN;
    - OBSERVE VARIATION OF OCEAN RADAR CROSS SECTION USING ANGLE OF INCIDENCE, POLARIZATION AND LOOK DIRECTION.
  - PROCESSING REQUIREMENTS: PERFORM EIGHT-256 POINT FOURIER TRANSFORMS DURING 17 MILLISECONDS BETWEEN RADAR PULSES. 16 BIT ACCURACY, 8 BIT DATA SAMPLES.
- ARRAY PROCESSOR FOR NSCAT (FIGURE 2)
  - MODEST PROCESSING REQUIREMENT: 256 POINT FFT, 400 NS/BUTTERFLY.

$$(8 \text{ PASSES})\left(\frac{256}{2} \times \frac{\text{BUTTERFLIES}}{\text{PASS}}\right)\left(\frac{400 \text{ NS}}{\text{BUTTERFLY}}\right) \cong .4\text{MS FOR ONE 256 POINT FFT.}$$

$$8 - 256 \text{ POINT FFT: } (8)(.4\text{MS}) \cong 3.2 \text{ MS VS AVAILABLE } 17\text{MS.}$$

- INCORPORATION OF ALGORITHM IMPROVEMENT:
  - PROGRAMMABLE THEREFORE SOME FLEXIBILITY:
  - ABLE TO ACCOMMODATE CHANGES, E.G., ALGORITHM IMPROVEMENTS, MORE READILY.
  - ALLOWS FOR CALCULATION OF NEW SIGNAL STATISTICS NOT CURRENTLY REQUIRED FOR WIND MEASUREMENTS. EXAMPLE IS QUANTITIES WHICH CAN BE CALCULATED FROM RAW RADAR ECHO DATA, BUT WHICH COULD NOT BE CALCULATED FROM THE AVERAGED DATA THAT IS DOWNLINKED.

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PRELIMINARY BASELINE NROSS SCATTEROMETER FUNCTIONAL BLOCK DIAGRAM

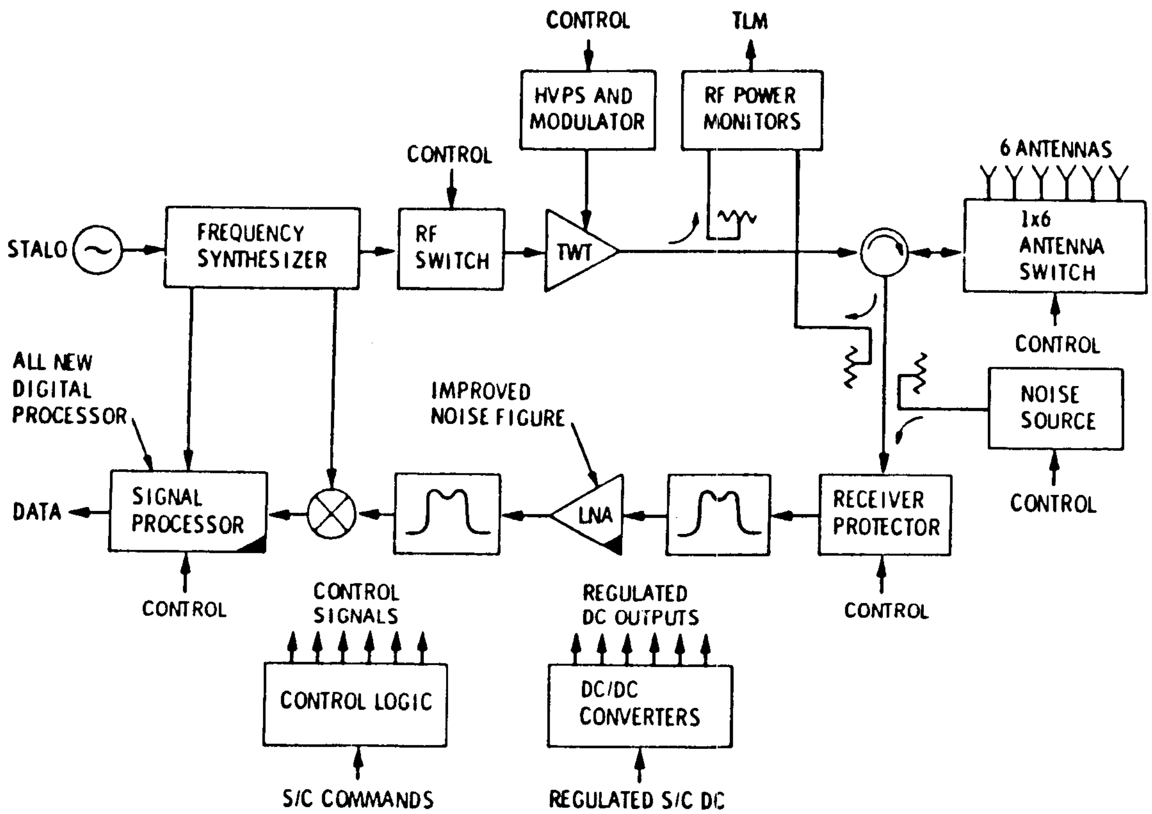

Figure 1. Functional block diagram for the NROSS wind measurement radar called NSCAT. The item discussed here is the signal processor at lower left.

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MP - AP SIGNAL PROCESSOR CONCEPT FOR NSCAT

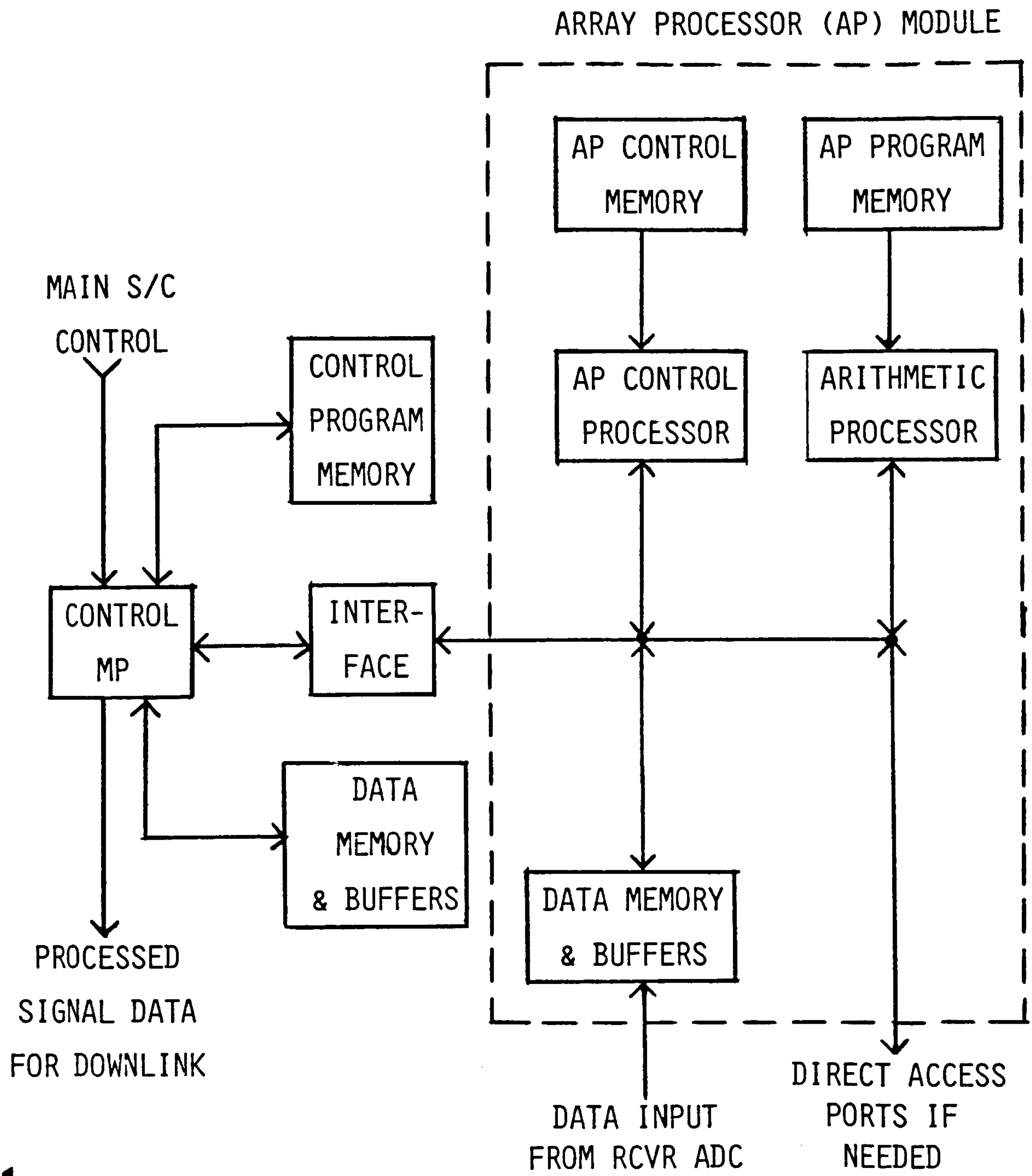

FIGURE 2. MICROPROCESSOR - ARRAY PROCESSOR (MP-AP) CONCEPT FOR THE NROSS WIND MEASUREMENT RADAR (NSCAT) SIGNAL PROCESSOR.

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DESIGN CONSIDERATION FOR FLIGHT ARRAY PROCESSORS

- ADSP (FIGURE 3) - STUDY CONTRACT WITH UNIVERSITY OF ARIZONA
  - EARTH OBSERVATION
  - PROCESSING REQUIREMENT (SIR-B AS BASELINE): APPROXIMATELY 1.5 GIGAFLOPS.
  - WESTINGHOUSE VSHIC COMPLEX ARITHMETIC VECTOR PROCESSOR CAPABLE OF 40 MILLION COMPLEX FFT BUTTERFLIES/SEC. (40 MCOPS).
  - 40 MCOPSX 10 $\frac{\text{FLOP}}{\text{BUTTERFLY}}$ = .4 GIGAFLOPS. LESS THAN 50 WATTS.
  - HUGE RAM - 160 MBYTES.
  - BLOCK OUT DESIGN.
  - POWER, WEIGHT, VOLUME, RADIATION HARDNESS, SEU.
  - KNOWING BOUNDS, HOW FEASIBLE IS IT?

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ADSP STATUS REPORT
HARDWARE BLOCK DIAGRAM

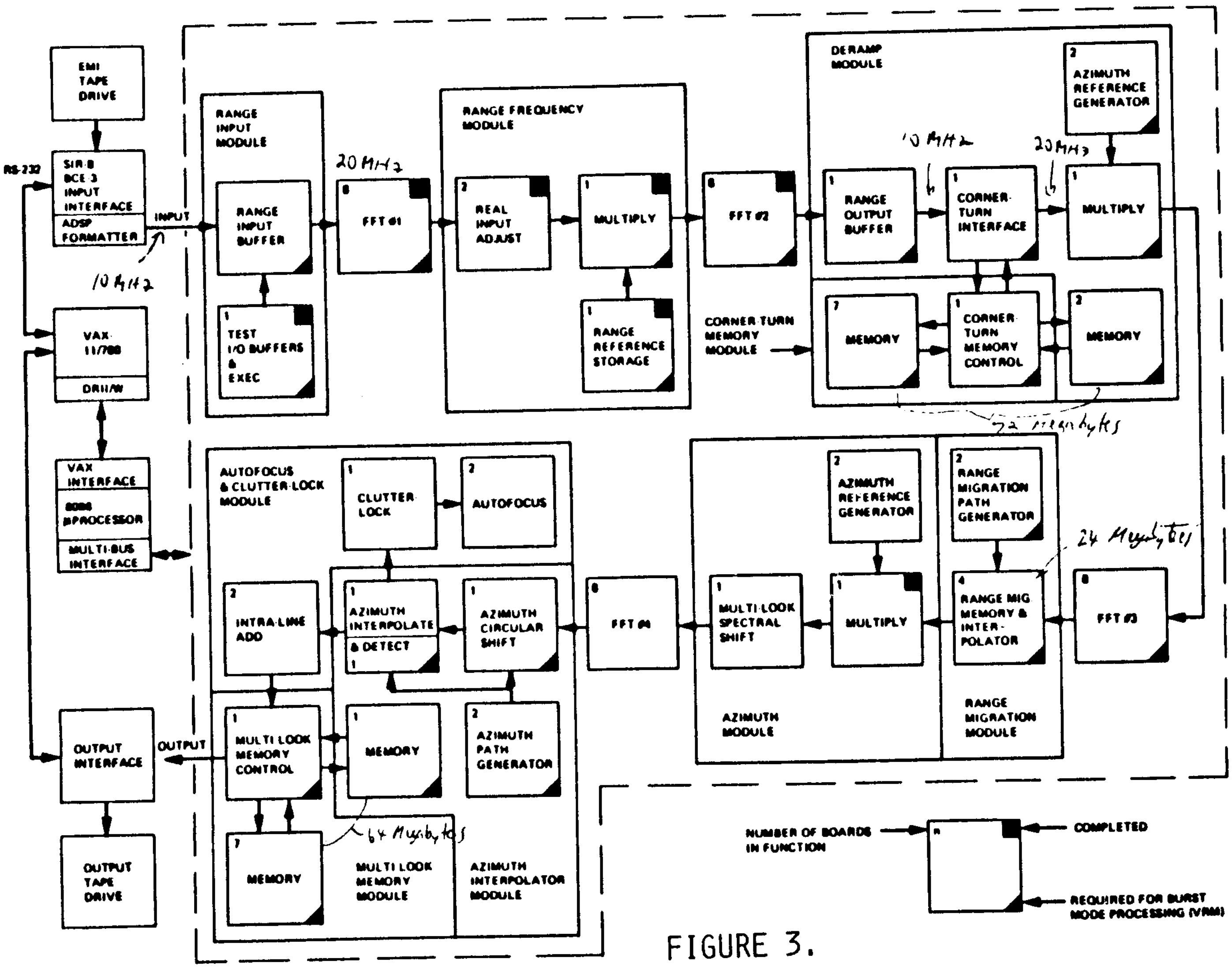

FIGURE 3.

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ISSUES REGARDING SPACEFLIGHT APPLICATIONS OF ARRAY PROCESSORS

- TRANSMISSION TO EARTH OF RAW VS. SPACECRAFT PROCESSED DATA.
  - IF LARGE AMOUNTS OF DATA (E.G., IMAGES OF THE EARTH) CAN BE COMPRESSED (FILTERED), COMMUNICATION COSTS ARE LOWERED. BUT CAN THE COMPRESSED DATA SATISFY THE USER?
- NEED FOR REAL TIME SIGNAL AND IMAGE PROCESSING ONBOARD SPACECRAFT.
  - SPACE STATION - CREW MEMBERS WOULD NEED REAL TIME SOLAR IMAGES TO ACTIVATE SOLAR FLARE OBSERVATIONS AS OCCURRED DURING SKYLAB. DOES CREW NEED REAL TIME INFORMATION TO CONTROL EXPERIMENTS AND OBSERVATIONS OR WILL THE CONTROL FUNCTION BE DONE ON GROUND VIA SPACECRAFT CONTROL CENTER (SPOCC)? IF THE CREW PLAYS AN IMPORTANT OR EXCLUSIVE ROLE, THEN SPACECRAFT ARRAY PROCESSORS COULD PLAY A VERY SIGNIFICANT ROLE IN PROVIDING NECESSARY REAL TIME DATA.
- COMPATIBLE BUS SPEEDS
  - EASY TO SEE A SEVERE BOTTLENECK WOULD DEVELOP IF A FAST ARRAY PROCESSOR INTERFACED TO A SPACECRAFT SYSTEM WITH INSUFFICIENT SPEED TO PROVIDE DATA TO OR ACCEPT OUTPUT FROM AN ARRAY PROCESSOR.
  - WORKING CLOSELY WITH JPL'S MAX HIGH SPEED COMPUTER DESIGN GROUP (I.E., MAX COULD BE THE HOST FOR THE ARRAY PROCESSOR).

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ISSUES REGARDING SPACEFLIGHT APPLICATIONS OF ARRAY PROCESSORS

(CONTINUED)

- TECHNOLOGY
  - VHSIC
  - SANDIA 32000
  - GaAs
  - OTHER

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N.D. MURRAY

INFORMATION NETWORK ARCHITECTURES

NASA/LARC

506-58-13

INFORMATION DATA SYSTEMS FOR ADVANCED AEROSPACE MISSIONS, SUCH AS SPACE STATION AND ITS CO-ORBITING PLATFORMS, ARE NEEDED THAT ARE EVOLVABLE, ADAPTIVE, AND FAULT TOLERANT. LOCAL AREA INFORMATION NETWORKS ARE CONSIDERED A MOST LIKELY TECHNOLOGY SOLUTION; ITS PRINCIPLE NEEDS ARE: 1) THAT INFORMATION FLOW BETWEEN DEVICES ON A NETWORK AND ITS CONTROL REQUIRES IMPROVEMENT, PARTICULARLY FOR MODERATELY OR TIGHTLY COUPLED HIGH PERFORMANCE PROCESSES; 2) THAT THE NETWORK SHOULD POSSESS FAULT TOLERANT PROPERTIES TO MEET SAFETY RELATED CRITICALITIES; AND 3) THAT HIGH PERFORMANCE (>100 MBPS) IS REQUIRED IF SPACE STATION IS TO HAVE AN INTEGRATED SYSTEM DATA NETWORK FORM WHERE VIDEO, VOICE, AND DATA ARE TO BE SIMULTANEOUSLY ACCOMMODATED. THE BRAIDED MESH FORM OF NETWORK HELPS MEET THESE NEEDS WITH THE FOLLOWING FEATURES: 1) SIMULTANEOUS ADAPTABLE DATA COMMUNICATION LINKS OFFERS DYNAMIC AND HIGH PERFORMANCE ACCOMMODATION, AND 2) ALTERNATE COMMUNICATION LINKS PROVIDE A CAPABILITY FOR SELF-CORRECTING AND REPAIRING (OR FAULT TOLERANT) PROPERTIES. ALSO, THE HIGH PERFORMANCE REQUIREMENT LEADS TO THE CONCEPT OF A NETWORK THAT USES FIBER OPTICS LINKS AND OPTICAL NODES; FIBER OPTICS WITH WAVELENGTH DIVISION MULTIPLEXING WOULD BE USED.

THIS EFFORT IS TO RESEARCH AND CHARACTERIZE THE ARCHITECTURAL ISSUES OF THE BRAIDED MESH FORM OF NETWORK, AND ALSO TO DEVELOP AN OPTICAL NODE WHICH WOULD FORM THE USER INTERFACE INTO THE NETWORK, CONTROL USER ACCESS TO THE NETWORK, PROVIDE ADAPTABLE MULTIPLE PATH DATA COMMUNICATIONS FROM/TO OTHER NODES, AND PROVIDE FOR OVERALL CONTROL OF THE NETWORK. SUCH A NODE NEEDS A MEANS OF LOW LOSS OPTICAL SWITCHING, WHICH IS CURRENTLY BEING DEVELOPED THROUGH INTEGRATED OPTICS. FUTURE EFFORTS WOULD BE TO CONSTRUCT A LABORATORY HIGH PERFORMANCE NETWORK, POPULATE IT WITH HIGH PERFORMANCE NETWORK USER DEVICES, AND EVALUATE/CHARACTERIZE THE NETWORK.

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INFORMATION NETWORK ARCHITECTURES

506-58-13/N. MURRAY

OBJECTIVE

INFORMATION NETWORK ARCHITECTURE - RESEARCH AND DEVELOP INFORMATION NETWORKS TO MEET THE SPACE STATION NEEDS OF SELF-CORRECTING AND REPAIRING, HIGH PERFORMANCE, EVOLVABILITY, ADAPTABILITY, SECURITY, AND EFFICIENCY.

APPROACH

- RESEARCH, EVALUATE AND CHARACTERIZE THE ARCHITECTURAL TYPE NETWORKS.
  - CENTRAL CONTROL, STATIC, SELF CORRECTING/REPAIRING (MESH)
  - DISTRIBUTED CONTROL, ADAPTIVE, SELF CORRECTING/REPAIRING (MESH)

C. S. DRAPER LABS RTI/NORTH CAROLINA STATE UNIVERSITY UNIVERSITY OF ILLINOIS, URBANNA	IN-HOUSE EMULATION

- RESEARCH AND DEVELOP AN ADAPTIVE OPTIC NODE:

- OPTIC X-SWITCH TEST ARTICLE	BATTELLE MEMORIAL INST.
- INTERMEDIATE OPTIC NODE	HONEYWELL INC.
- FINAL OPTIC NODE	

- RESEARCH, EVALUATE AND CHARACTERIZE A HIGH PERFORMANCE, ADAPTIVE, OPTICAL NODE TYPE NETWORK. (FOCUSED TECHNOLOGY PROPOSAL)

MANNED SPACE STATION

REQUIREMENTS FOR INFORMATION PROCESSING	CRITICALITY	PERFORMANCE
1. EXPERIMENTS AND MANUFACTURING	HIGH	MODERATE
2. OBSERVATIONS	HIGH	HIGH
o EARTH o NEAR EARTH o SOLAR SYSTEM o DEEP SPACE		
3. COMMUNICATIONS	HIGH	MODERATE
4. CONSTRUCTION	HIGHER	HIGH
5. STABILITY AND CONTROL	HIGHEST	MODERATE
6. AUTONOMY/AUTOMAINTENANCE	HIGHEST	MODERATE
7. HOUSEKEEPING	HIGHEST	MODERATE

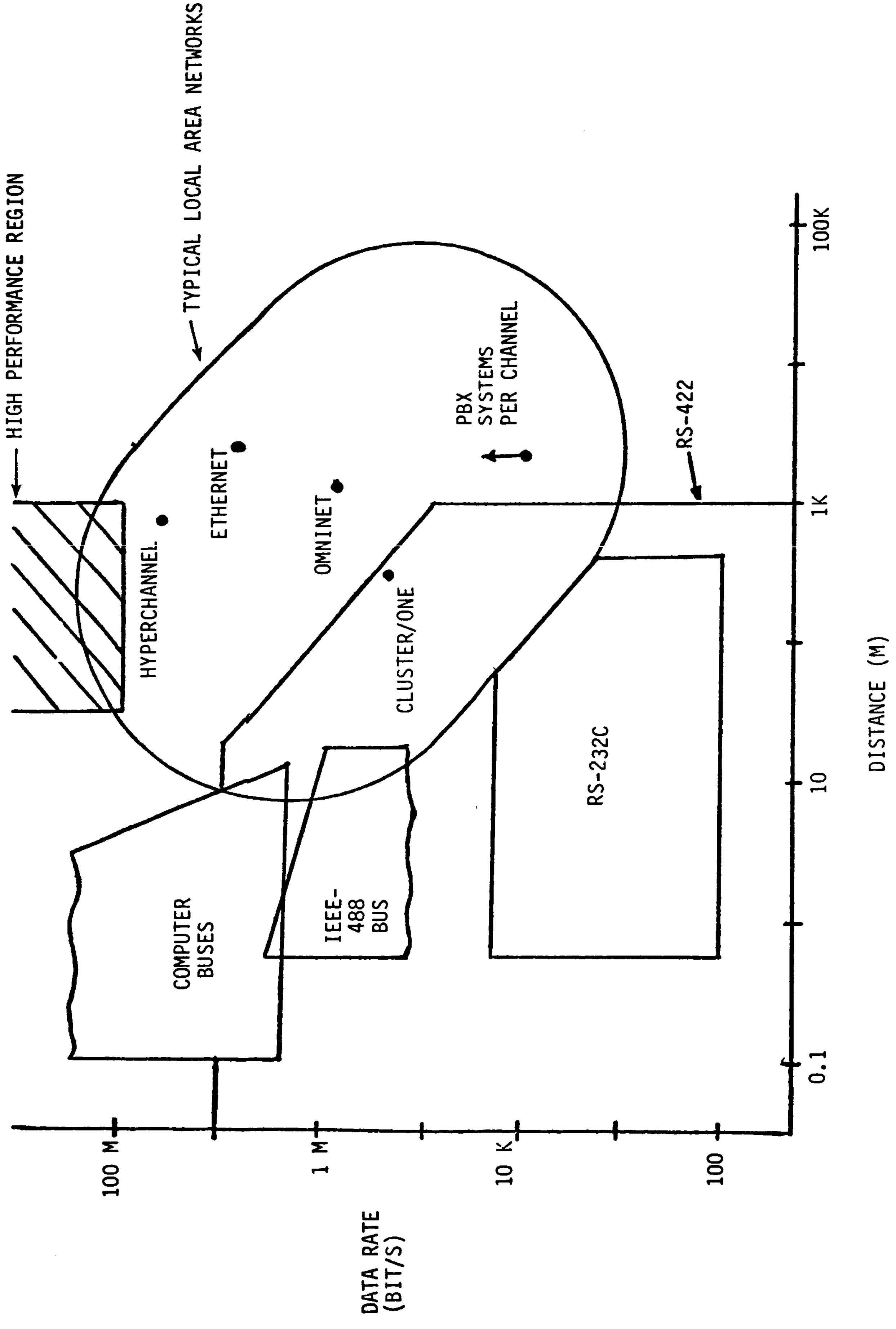
CRITICALITY - HIGHEST IMPLIES MAN RATED OR SPACECRAFT RATED SAFETY.
HIGH IMPLIES HIGH COST BUT NOT SAFETY RELATED.

PERFORMANCE - COMMUNICATION
- MODERATE ~ 50 MBPS
- HIGH > 100 MBPS

PROCESSING
- MODERATE ~ 10 MOPS
- HIGH > 50 MOPS

SUMMARY CHARACTERISTICS OF DATA TRAFFIC SOURCES

TRAFFIC TYPE	NDM. MESSAGE LENGTH (BITS)	RATE BPS	CALL GEN. RATE	HOLDING TIME	DELAY REQUIRE.
STREAM VOICE	CONTINUOUS	64K	LOW	LONG	ALMOST INSTANTANEOUS
STREAM DATA	CONTINUOUS	64K	LOW	LONG	VARIABLE
INTERACTIVE DATA	HUNDREDS TO THOUSANDS	64K	HIGH	SHORT	FRACTION SEC. TO SECONDS
INQUIRY/ RESPONSE DATA	HUNDREDS TO THOUSANDS	64K	LOW	SHORT	SECONDS TO MINUTES
DATA BASE UPDATE	HUNDREDS	TBD	LOW	SHORT	SECONDS TO MINUTES
BULK DATE TRANSFER	GREATER THAN 10^4	TBD	LOW	MED TO LONG	SECONDS TO HOURS
DIGITAL VIDEO	CONTINUOUS	100M	LOW	LONG	ALMOST INSTANTANEOUS


HIGH PERFORMANCE REGION
TYPICAL LOCAL AREA NETWORKS
HYPERCHANNEL
ETHERNET
OMNINET
CLUSTER/ONE
PBX SYSTEMS PER CHANNEL
RS-422
RS-232C
COMPUTER BUSES
IEEE-488 BUS
100 M
1 M
10 K
100
DATA RATE (BIT/S)
0.1
10
1K
100K
DISTANCE (M)

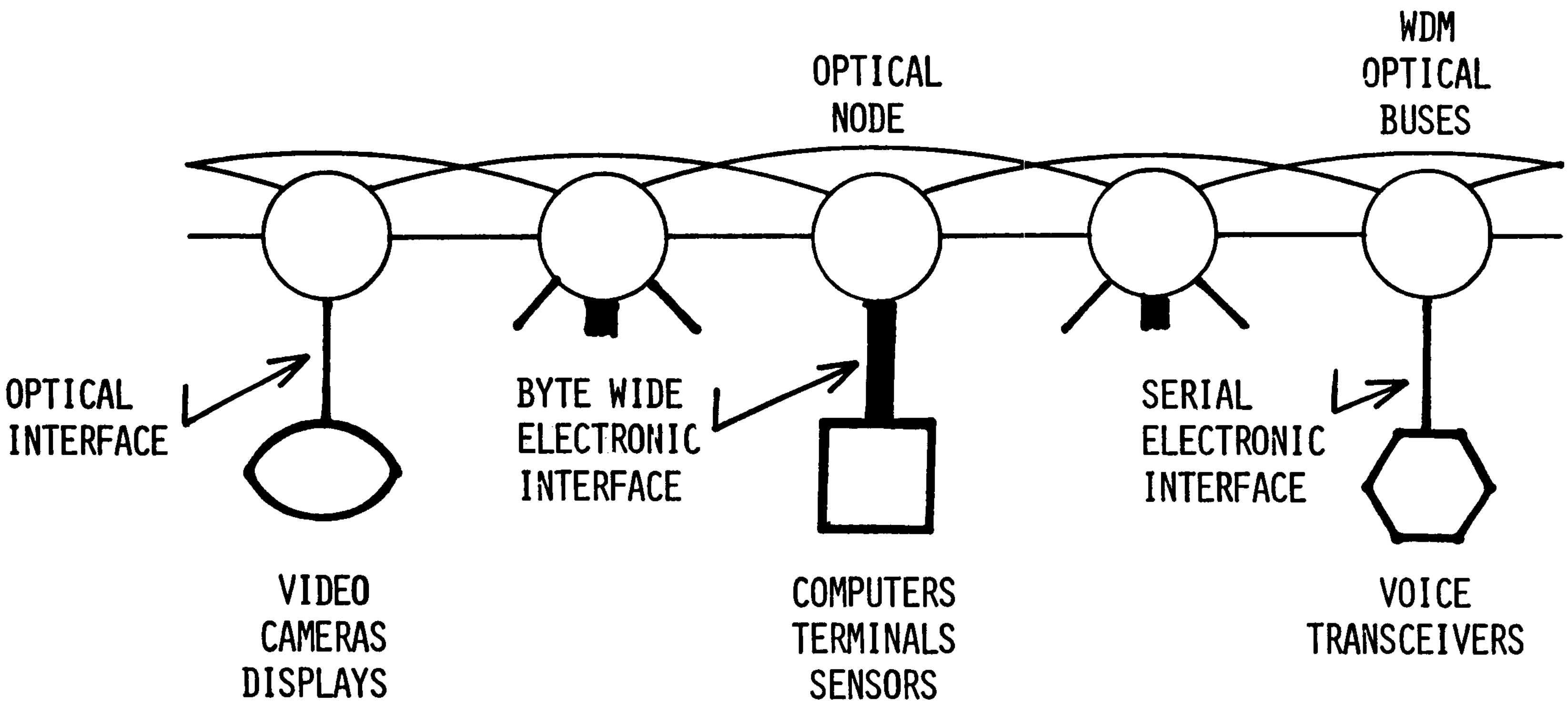
INFORMATION NETWORK ARCHITECTURES

506-58-13/N. MURRAY

- INTEGRATED - DATA, VOICE, VIDEO
- KEY ISSUES OF NETWORKS
  - INFORMATION FLOW/OPERATING SYSTEM (SEPARATE DATA, CONTROL COMMUNICATIONS)
  - SELF-CORRECTING AND REPAIRING/FAULT TOLERANCE (MESH TOPOLOGY)
  - HIGH PERFORMANCE (FIBER OPTICS/INTEGRATED OPTICS, MESH TOPOLOGY)

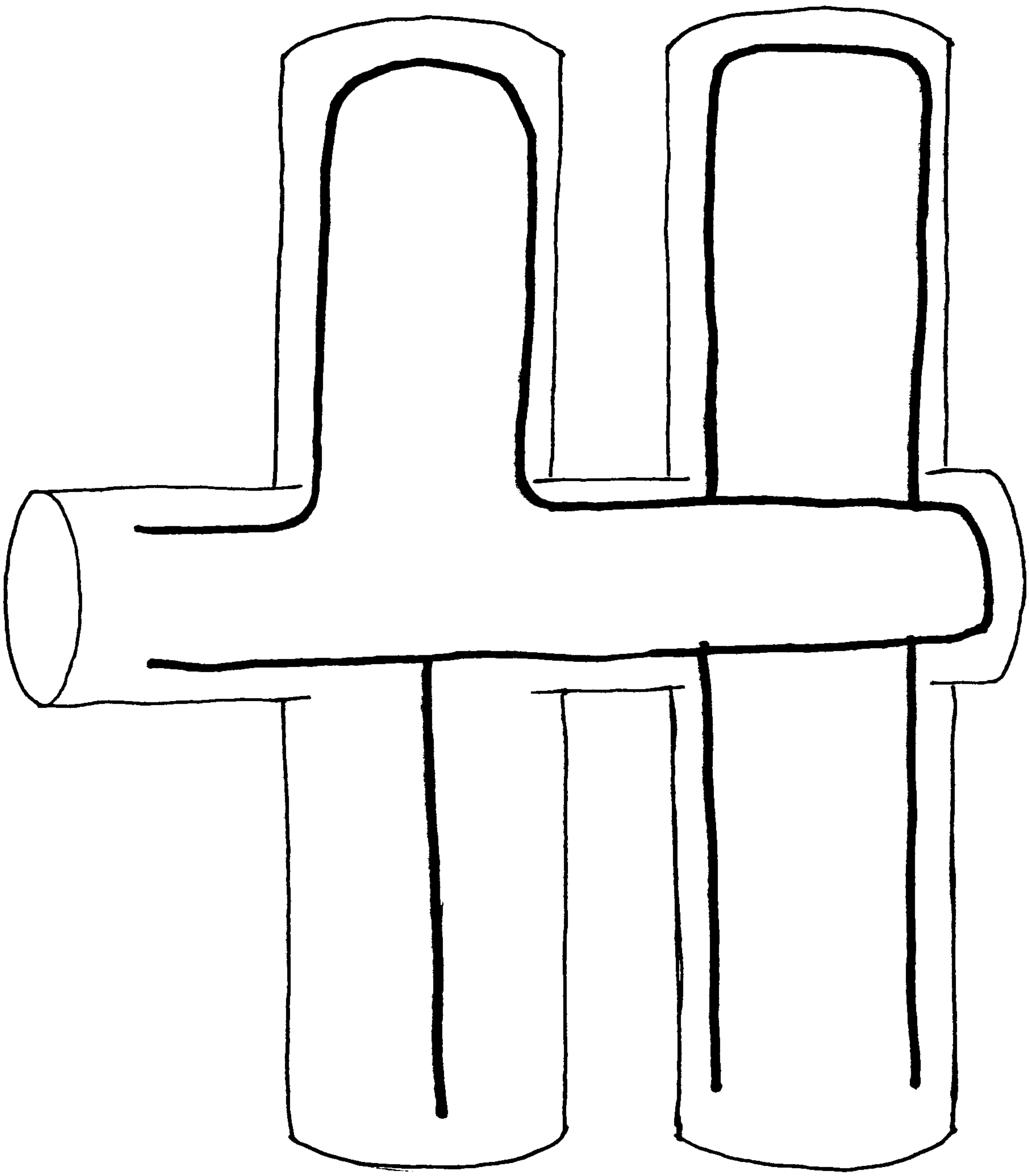
INFORMATION FLOW BETWEEN COMPUTERS AND OTHER DEVICES REQUIRES A SYSTEM AND ARCHITECTURAL SOLUTION THAT AFFECTS BOTH HARDWARE AND SOFTWARE. CURRENT SYSTEMS USE EXTENSIVE SOFTWARE FOR THE INFORMATION FLOW RESULTING IN A SOFTWARE BOTTLENECK; CONTROL ALGORITHMS AND METHODS FOR TIGHTLY COUPLED, HIGH PERFORMANCE, DISTRIBUTED PROCESSING ARE INADEQUATE; SELF CORRECTING AND REPAIRING TECHNIQUES ARE NOT BEING FULLY APPLIED TO TODAY'S SYSTEMS. REAL-TIME, FULL MOTION, DIGITAL COLOR VIDEO REQUIRES DATA RATES IN EXCESS OF 100 MBPS.

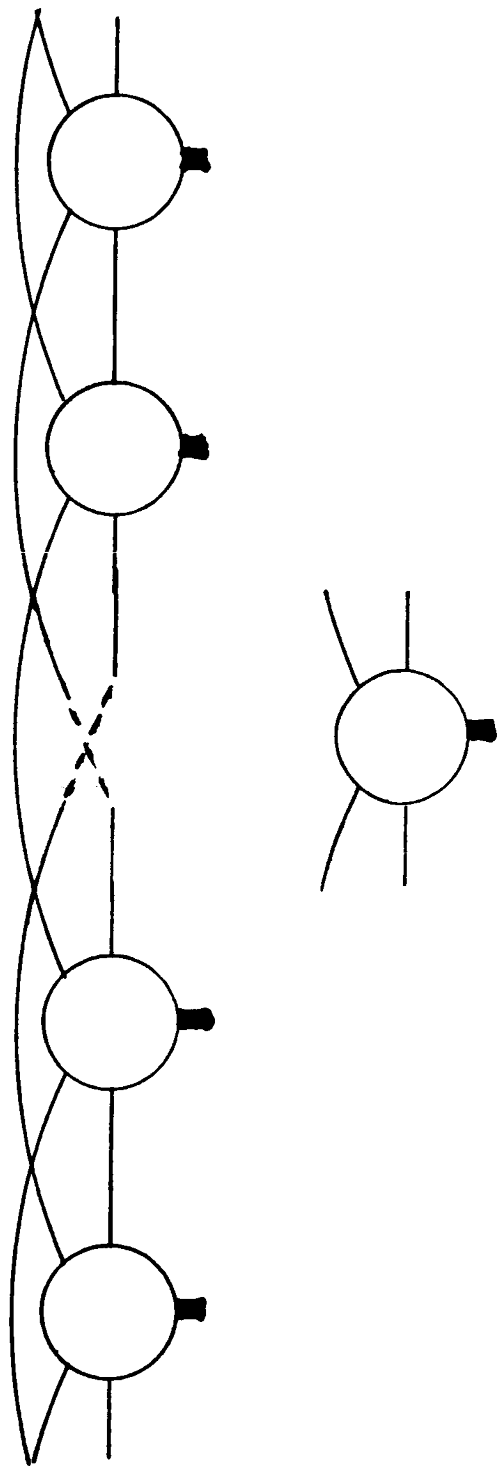
NETWORK ARCHITECTURE/TOPOLOGY



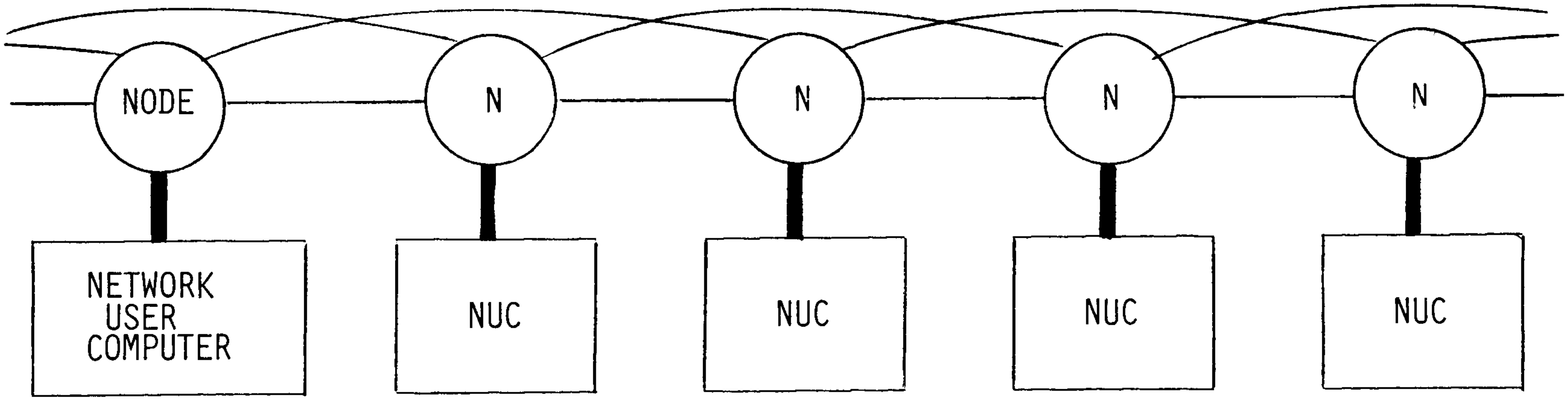
o HIGH PERFORMANCE o

o FAULT TOLERANT o





ELECTRONIC EMULATION OF OPTIC NETWORK

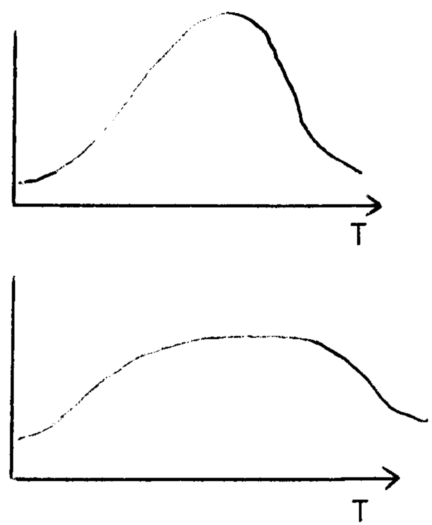


DATA ACCUMULATION
- EVENTS
- TIME

STATISTICAL EVALUATIONS

USER SERVICE DEMAND

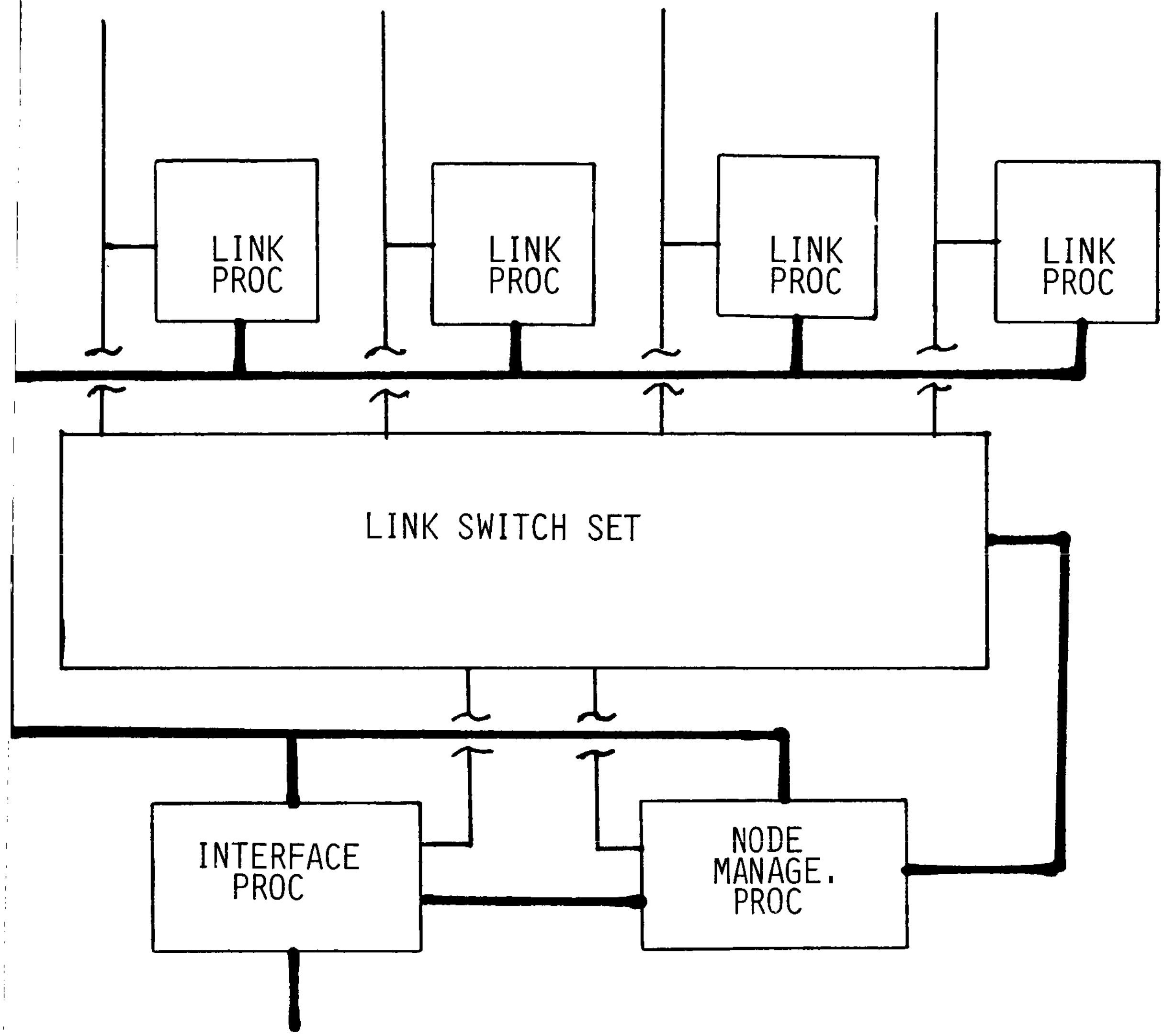
USER SERVICE TIME



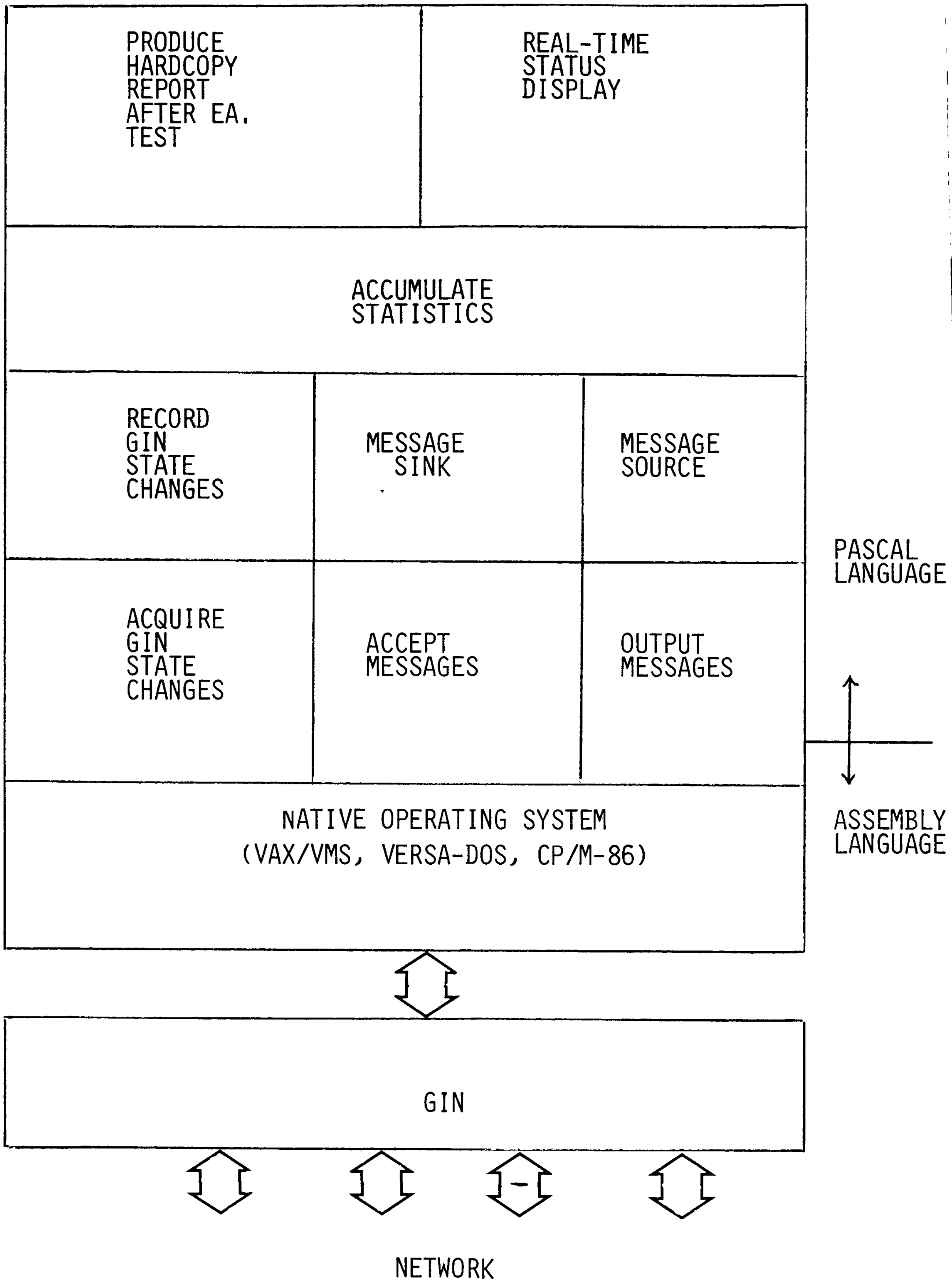
PARAMETRICALLY CONTROLLED DISTRIBUTIONS

EVALUATION OF:
- FAILURE DETECT/ RECOVER
- CENTRALIZED ROUTING
- DISTRIBUTED ROUTING
- FLOW CONTROL
- NETWORK UTILIZATION
- NUC/NODE INTERFACES

EMULATION NODES



ALL PROCESSORS MOTOROLA M68K


PRODUCE HARDCOPY REPORT AFTER EA. TEST
REAL-TIME STATUS DISPLAY
ACCUMULATE STATISTICS
RECORD GIN STATE CHANGES
MESSAGE SINK
MESSAGE SOURCE
PASCAL LANGUAGE
ACQUIRE GIN STATE CHANGES
ACCEPT MESSAGES
OUTPUT MESSAGES
ASSEMBLY LANGUAGE
NATIVE OPERATING SYSTEM (VAX/VMS, VERSA-DOS, CP/M-86)
GIN
NETWORK

ROUTING ALGORITHMS

1) NON-ADAPTIVE

   - NO ATTEMPT TO ADJUST TO CHANGING NET CONDITIONS
   - FIXED OR RANDOM ROUTING

2) CENTRALIZED ADAPTIVE

   - CENTRAL AUTHORITY DICTATES ROUTING DECISIONS
   - MORE NEAR OPTIMAL ROUTING
   - ROUTING CONTROL CENTER CAN REPRESENT PERFORMANCE BOTTLENECK

3) ISOLATED ADAPTIVE

   - INDEPENDENT OPERATION
   - ADAPTABILITY VIA EXCLUSIVE USE OF LOCAL NODE DATA

4) DISTRIBUTED ADAPTIVE

   - UTILIZE INTERNODE COOPERATION
   - NODES EXCHANGE INFORMATION TO ARRIVE AT ROUTING DECISIONS

-McQUILLAN, BBN

PATH SEARCH ALGORITHM

Purpose

1. Routing data through a meshed network
2. Establishing a circuit set up
3. Adaptive to topological changes
4. Simultaneous communication desirable

8501B364-4

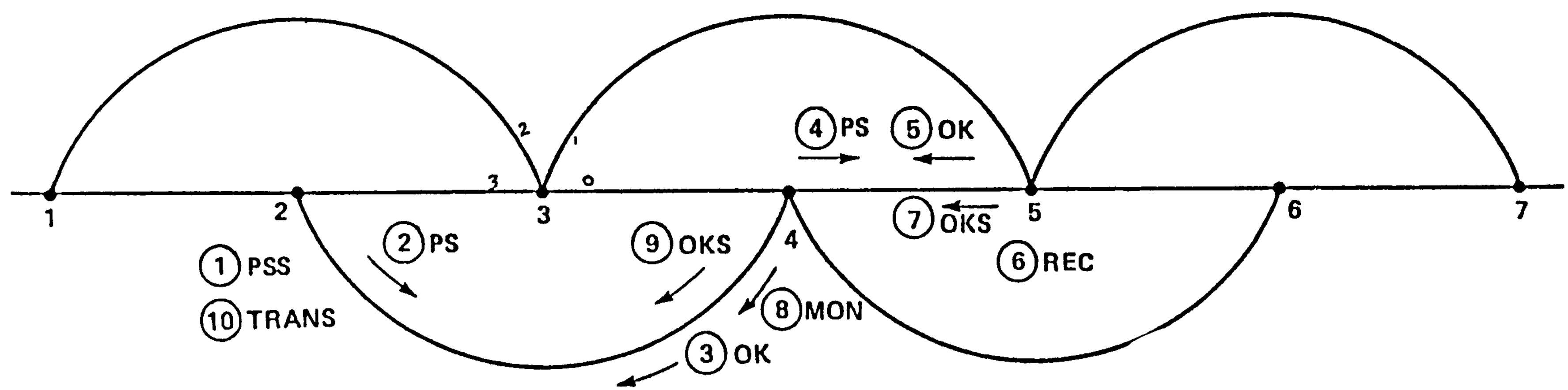
ROUTING ALGORITHM

Example: for node 3

DESTINATION NODE

Link Priority	1	2	3	4	5,6,7
1	LP 2 → 1	LP 3 → 2	–	LP 0 → 4	LP 1 → 5
2	LP 3 → 2	LP 2 → 1	–	LP 1 → 5	LP 0 → 4
3	LP 0 → 4	LP 0 → 4	–	LP 3 → 2	LP 3 → 2
4	LP 1 → 5	LP 1 → 5	–	LP 2 → 1	LP 2 → 1

EX 1: NORMAL OPERATION



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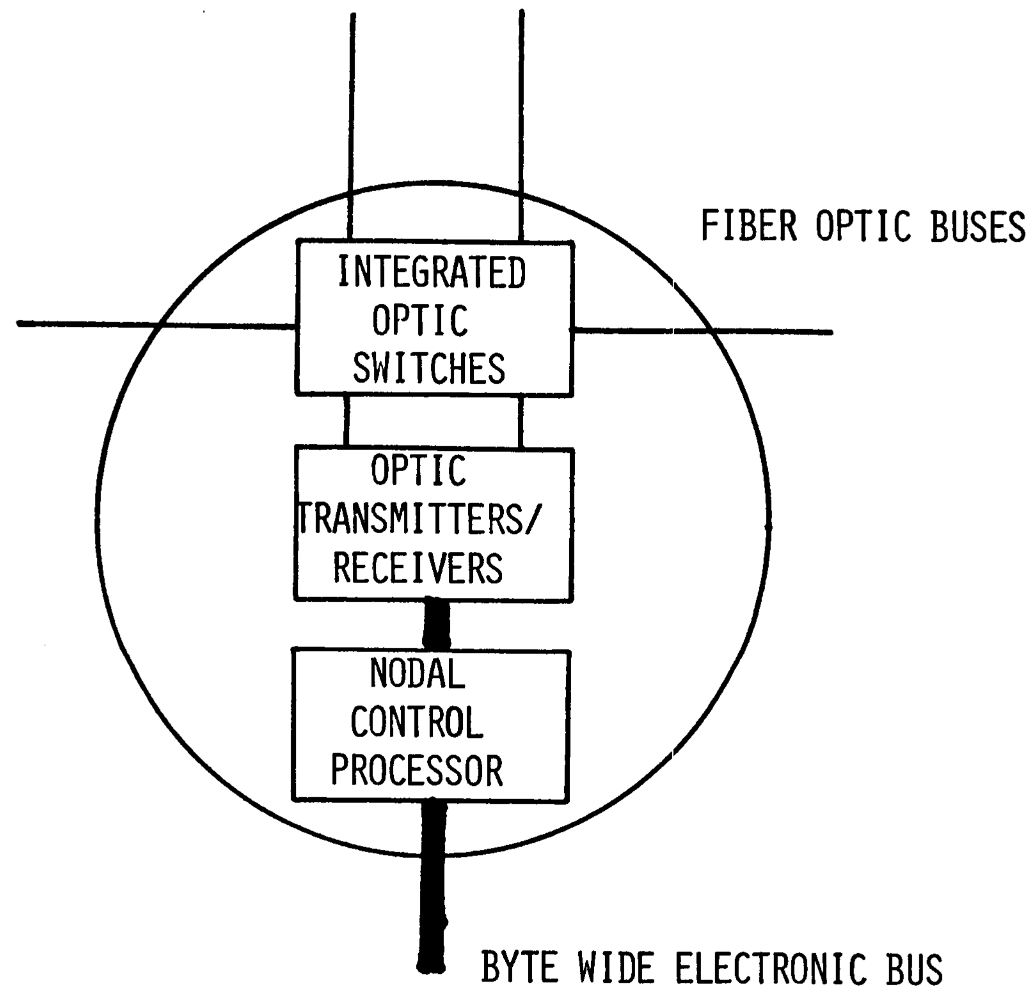
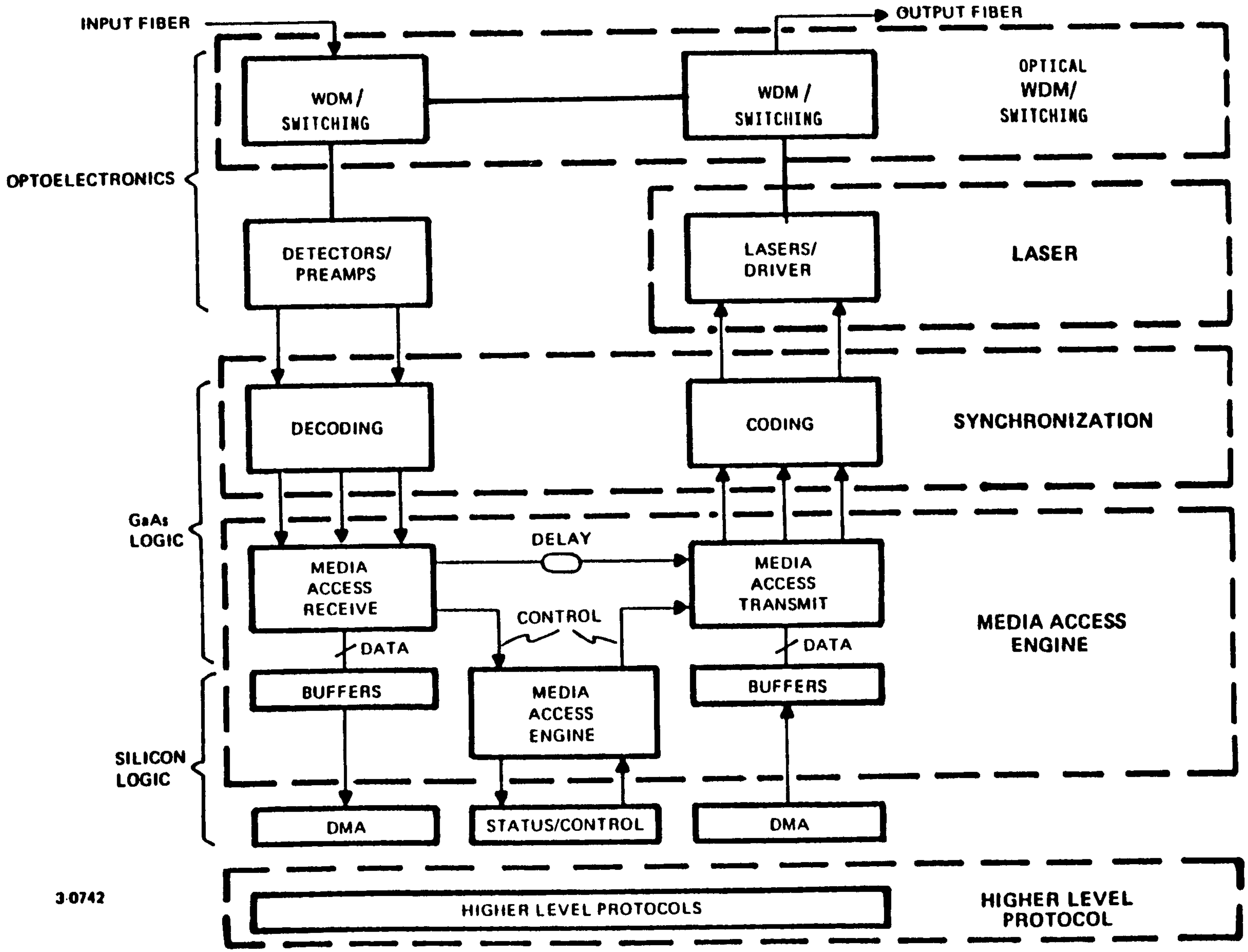


ADAPTIVE NODE DEFINITION

TECHNOLOGY PARTITIONING OF NODE INTERFACE UNIT



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INTELLIGENT OPTIC NODE TECHNOLOGY TIMELINE

FUNCTIONS \ TIME	NEAR TERM (1-2 YEARS)	MEDIUM TERM (3-5 YEARS)	LONG TERM (5-10 YEARS)
• E/O	GaAlAs (discrete)	GaAlAs with drive/ detector electronics	Monolithic GaAs
• O/E	Si		
• Fiber	Single mode, non-polarization preserving		polarization preserving?
• Taps, Delay	Fiber	SAW	TBD
• Amplification	Si	GaAs	Monolithic GaAs
• Switching	$LiNbO_3$ (bulk)	$LiNbO_3$ / ZnO ?	ZnO? / ALGaAs
• Synchronization	Si / GaAs	GaAs (discrete)	Monolithic GaAs
• Frame/Address Recognition	Fiber / GaAs	SAW / GaAs	TBD
• Conflict Resolution	Si / GaAs	GaAs	Monolithic GaAs
• Routing	N/A	Si / GaAs (d[illegible]	
• Higher Level Protocols		Si	

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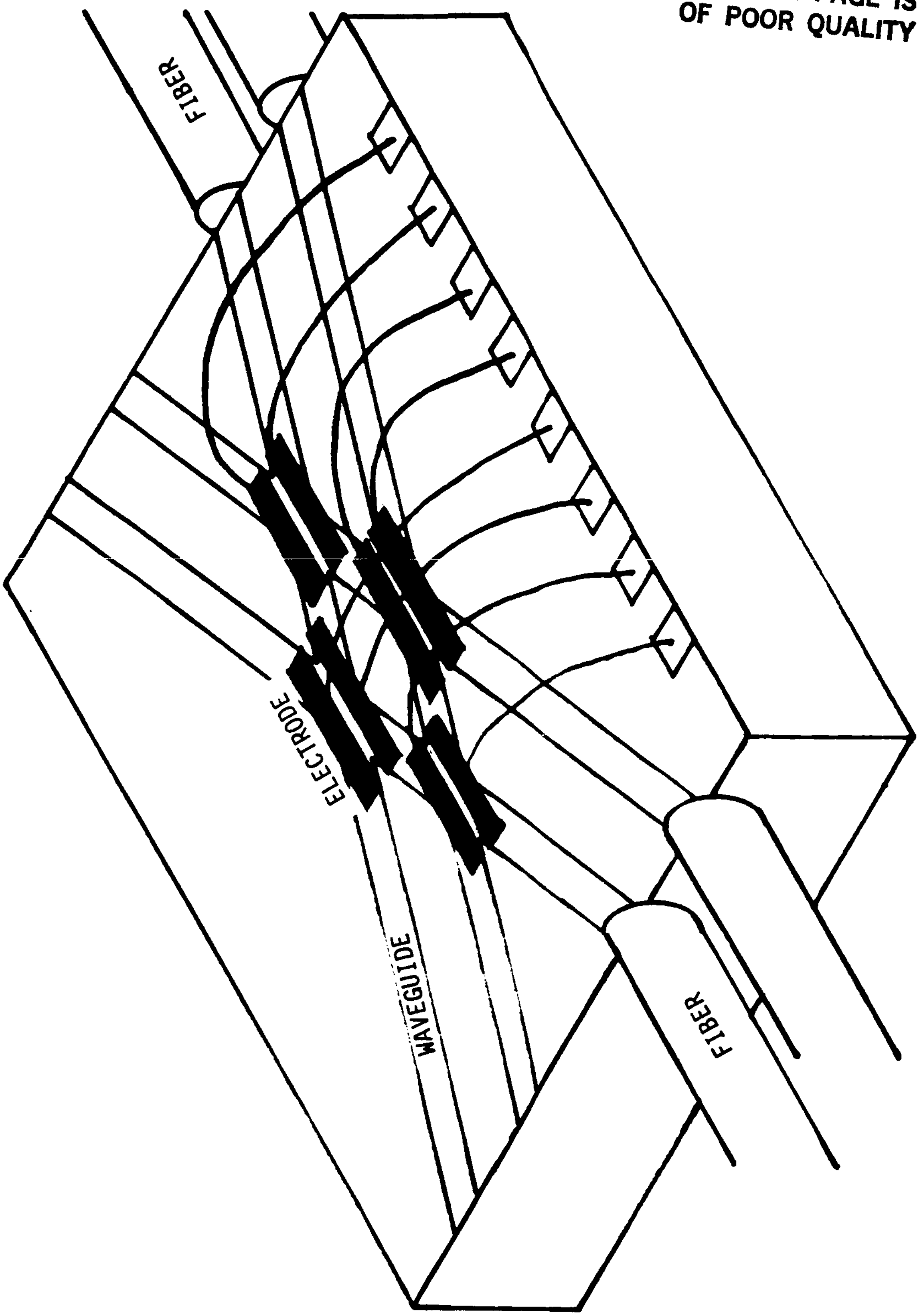
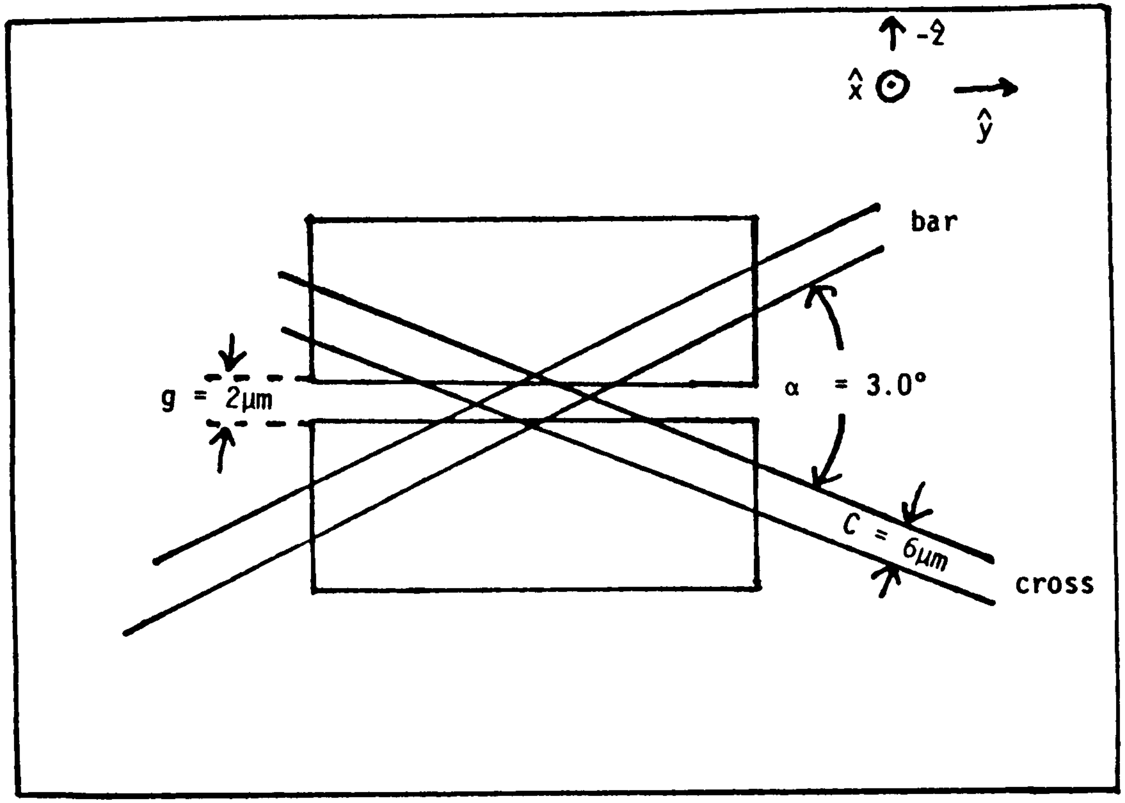
SOURCE MATERIALS

MATERIALS	GaAs/GaAlAs	InGaAsP	AlInGaAs	InGaAs	GaN	GaAsP
EMISSION WAVELENGTH	.82-.9 μm	1.0-1.6 μm	1.0-20 μm	3.3-3.8	.4 μm	VISIBLE
LASERS	X	X	X	NO	NO	NO?
LED's	X	X	X	X	X?	X
INTEGRATABLE	YES	YES	YES		NO	NO
WITH ELECTRONICS	GaAs	InPor InGaAs (LOW LEVEL)			NO	NO
EASE OF FABRICATION	MATURE	ALMOST MATURE LPE GROWTH	EXPERIMENTAL MBE/MOLVD	NEXT TO IMPOSSIBLE LPE	CONCEPTUAL	MATURE VPE



SCHEMATIC OF 2 x 2 SINGLE-MODE SWITCH

OPTICAL SWITCH DEVELOPMENT



Voltage	bar	cross
0 volts	40	60
+40 volts ($-\hat{z}$ is +)	90	10
-20 volts	10	90
-40 volts	40	60

X-SWITCH LOSS ESTIMATES

	POLARIZATION PRESERVING FIBER	SINGLE MODE FIBER	MULTI MODE FIBER
INPUT	0.5	3.5	?
CROSS[1]	0.1	0.1	0.1
BAR[2]	0.2[3]	0.2[3]	0.2[3]
WAVEGUIDE	0.5	0.5	0.5
OUTPUT	0.5	0.5	0.5
TOTAL	1.8 DB	4.8 DB	1.3 + X[4]

(1) A SWITCH IN CROSS STATE
(2) A SWITCH IN THE BAR STATE
(3) TOTAL EXCESS LOSS
(4) X IS UNBOUNDED; COULD BE TIME DEPENDENT

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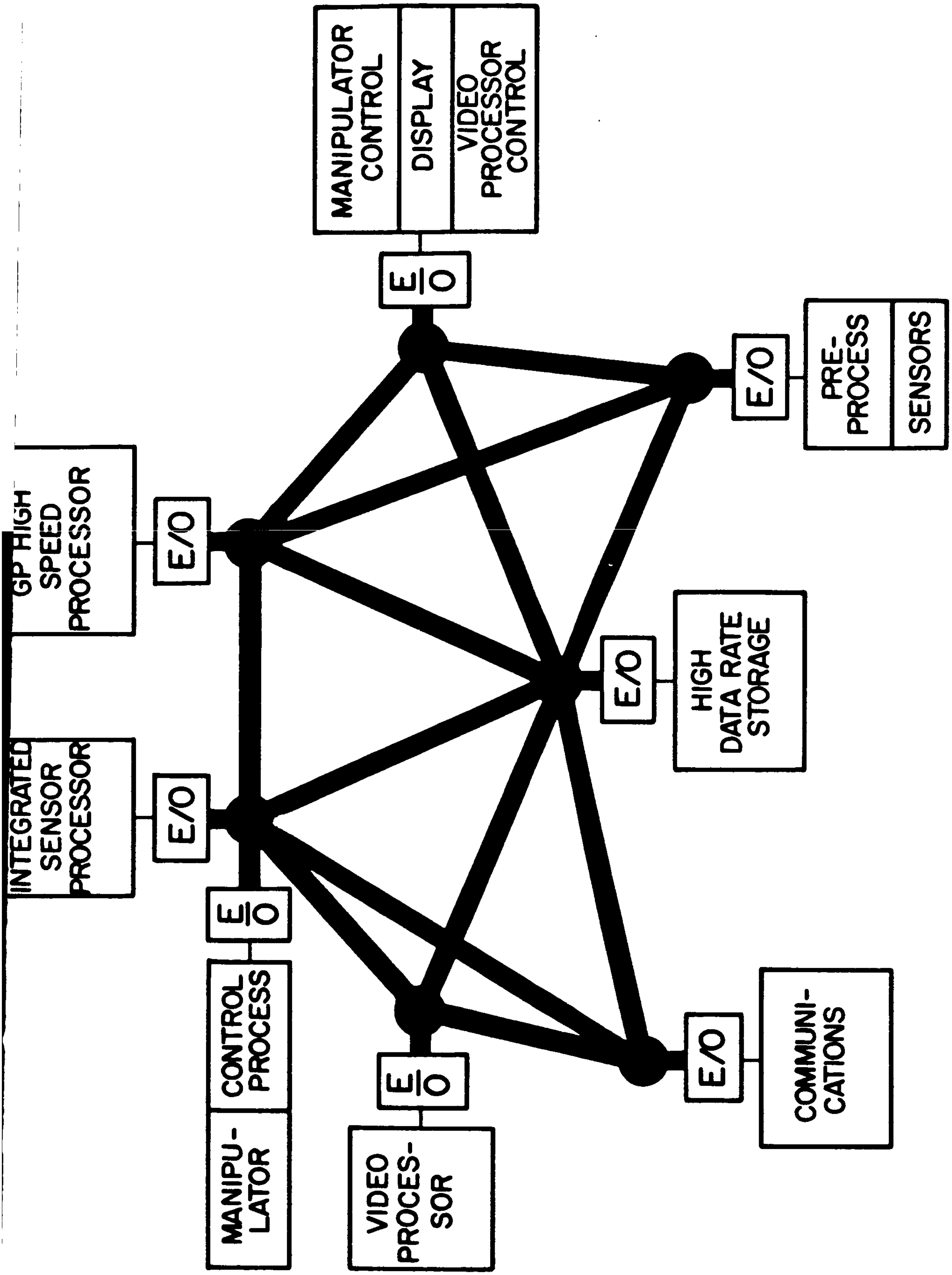
COMMON FEATURES FOR ALTERNATIVE DISTRIBUTED OPTICAL SWITCHING ARCHITECTURES

	FUNCTIONS \ ARCHITECTURE	LINEAR/STAR BUS	RING BUS	CIRCUIT SWITCH MESH	PACKE SWITC MESH
PHYSICAL LAYER	TRANSMITTER/ RECEIVER	BURST ASYNC	SYNCHRONOUS	BURST ASYNC	
	SWITCH	NO	COMMON FEATURES		
	COUPLER				
	CHANNELIZATION (WDMUX-WDDMUX)				
	AMPLIFIER				
	DELAY				
DATA LINK	ADDRESS COMPARE				
	CONFLICT RESOLUTION			SLOW	FAST
	ROUTING/GATEWAY				
HIGH LEVEL PROTOCOL	HI LEVEL PROTOCOL	RING OR STAR COMMON.		MINIMAL	SIMILAR TO RING OR STAR

TABLE (1)



[EXAMPLE HIGH PERFORMANCE NETWORK]

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N. D. MURRAY

VIDEO IMAGE PROCESSING

NASA/LARC

SPACE STATION WILL HAVE REQUIREMENTS FOR CONDUCTING SUCH MANIPULATION/OBSERVATION ACTIVITIES AS CONSTRUCTION, MAINTENANCE, MANUFACTURING, EXPERIMENTS, RENDEZVOUS AND DOCKING, POINTING AND TRACKING, TARGET ACQUISITION/IDENTIFICATION, AND SOLAR SYSTEM OBSERVATIONS. INITIALLY, MOST OF THESE MANIPULATIONS/OBSERVATIONS WILL REQUIRE A MAN-IN-THE-LOOP WITH VIDEO DISPLAY, WHICH IN TURN WILL REQUIRE REAL-TIME PROCESSING OF DATA AND INFORMATION FOR VISUAL PRESENTATION WILL IMPROVE MAN'S OPERATIONAL CAPABILITIES. AS THE SPACE STATION MATURES, SOME OF THESE OPERATIONS WILL BECOME NEARLY AUTONOMOUS WITH MAN MONITORING, WHICH WILL CREATE AN ADDITIONAL NEED FOR REAL-TIME PROCESSING AT DATA RATES EXCEEDING 100 MBITS/SEC. PROCESSING AT SUCH HIGH RATES WILL MOST LIKELY BE ACCOMPLISHED BY SPECIAL PURPOSE COMPUTING IMPLEMENTING COMPUTATIONALLY SIMPLE ALGORITHMS. CURRENT TECHNOLOGY PROJECTIONS INDICATE THE LACK OF AVAILABILITY OF SUCH SPECIAL PURPOSE COMPUTING IN THE EARLY 1990S, AND NASA NEEDS TO ACCELERATE THIS TECHNOLOGY FOR APPLICATION TO SPACE STATION. POTENTIAL FUNCTIONS FOR VIDEO IMAGE SPECIAL PURPOSE PROCESSING ARE BEING INVESTIGATED, SUCH AS SMOOTHING, ENHANCEMENT, RESTORATION AND FILTERING, DATA COMPRESSION, FEATURE EXTRACTION, OBJECT DETECTION AND IDENTIFICATION, PIXEL INTERPOLATION/EXTRAPOLATION, SPECTRAL ESTIMATION AND FACTORIZATION, AND VISION SYNTHESIS. ALSO, ARCHITECTURAL APPROACHES ARE BEING IDENTIFIED AND A CONCEPTUAL DESIGN GENERATED. COMPUTATIONALLY SIMPLE ALGORITHMS WILL BE RESEARCHED AND THEIR IMAGE/VISION EFFECTIVENESS DETERMINED. SUITABLE ALGORITHMS WILL BE IMPLEMENTED INTO AN OVERALL ARCHITECTURAL APPROACH THAT WILL PROVIDE IMAGE/VISION PROCESSING AT VIDEO RATES THAT ARE FLEXIBLE, SELECTABLE, AND PROGRAMMABLE.

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NASA
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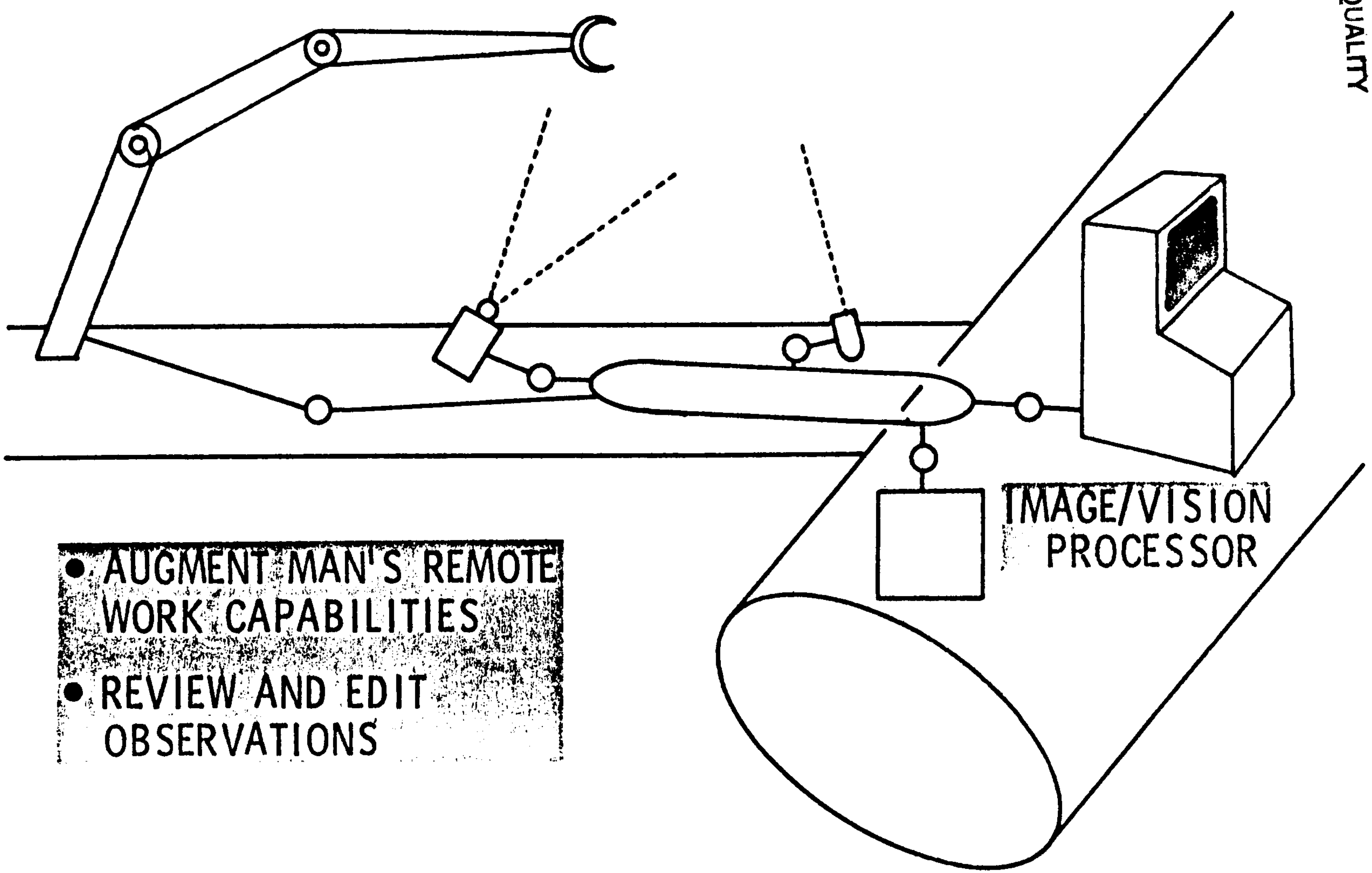
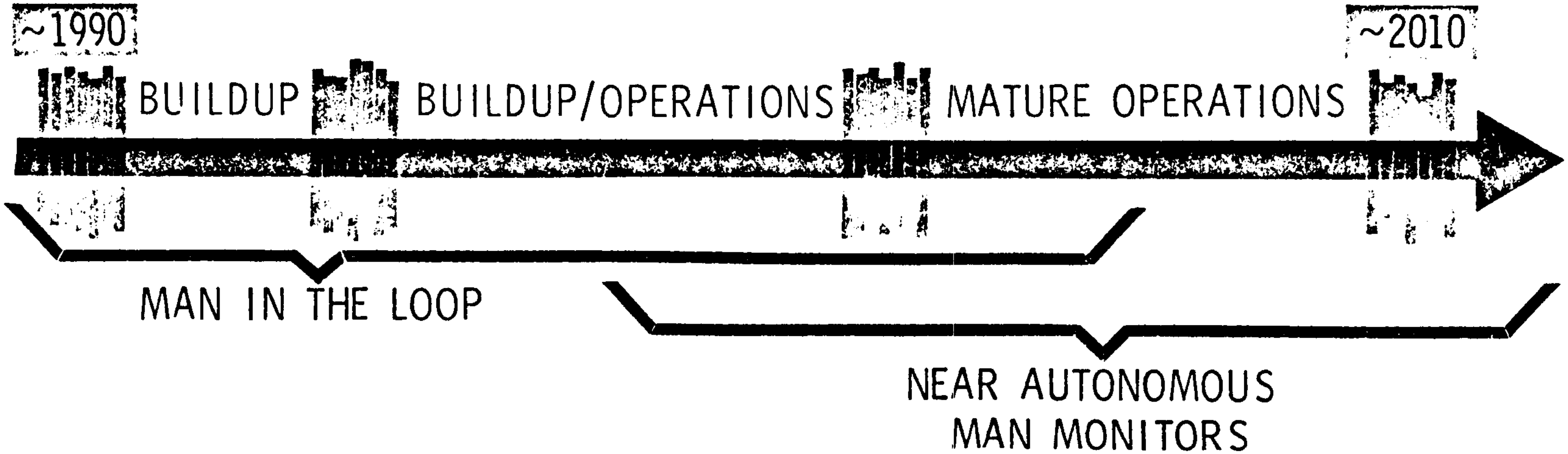
IMAGE/VISION PROCESSOR



- AUGMENT MAN'S REMOTE WORK CAPABILITIES
- REVIEW AND EDIT OBSERVATIONS

C-2

SPACE STATION EVOLUTION



MANIPULATIONS

- CONSTRUCTION
- MAINTENANCE
- MANUFACTURING
- EXPERIMENTS
- RENDEZVOUS AND DOCKING

OBSERVATIONS

- EARTH/SOLAR SYSTEM/DEEP SPACE
- MANUFACTURING
- EXPERIMENTS
- POINTING AND TRACKING
- TARGET ACQUISITION/IDENTIFICATION

SPACE STATION ACTIVITIES NEEDING VIDEO

- CONSTRUCTION
- SATELLITE SERVICING
- RENDEZVOUS
- PROXIMITY OPERATIONS
- COMMUNICATION AND TRACKING
- INSPECTION
- MAINTENANCE
- PAYLOAD DELIVERY/RETRIEVAL
- EXPERIMENT MONITORING
- DATA MANAGEMENT
- TRAINING

EXAMPLE SPACE STATION APPLICATIONS OF VIDEO IMAGE PROCESSING

RENDEZVOUS

- TARGET IDENTIFICATION
- TARGET TRACKING FOR CROSS RANGE VELOCITY AND POSITION ESTIMATION
- POINT TARGET DETECTION

PROXIMITY OPERATIONS

- TARGET TRACKING FOR TARGET ORIENTATION, POSITION AND VELOCITY ESTIMATION

DATA MANAGEMENT

- BANDWIDTH COMPRESSION FOR DATA MOVEMENT AND ARCHIVING

INSPECTION

- MACHINE VISION TECHNIQUES FOR VERIFICATION OF SPACE STATION STRUCTURAL INTEGRITY AND DETECTION AND CLASSIFICATION OF DEFECTS

COMMUNICATION AND TRACKING

- BANDWIDTH COMPRESSION FOR DOWNLINK TRANSMISSION
- MULTI-TARGET TRACKING FOR AREA TRAFFIC CONTROL
- TARGET DETECTION AND IDENTIFICATION FOR AREA TRAFFIC CONTROL

CONSTRUCTION

- VERIFICATION OF CONSTRUCTION STEPS

VIDEO IMAGE PROCESSOR

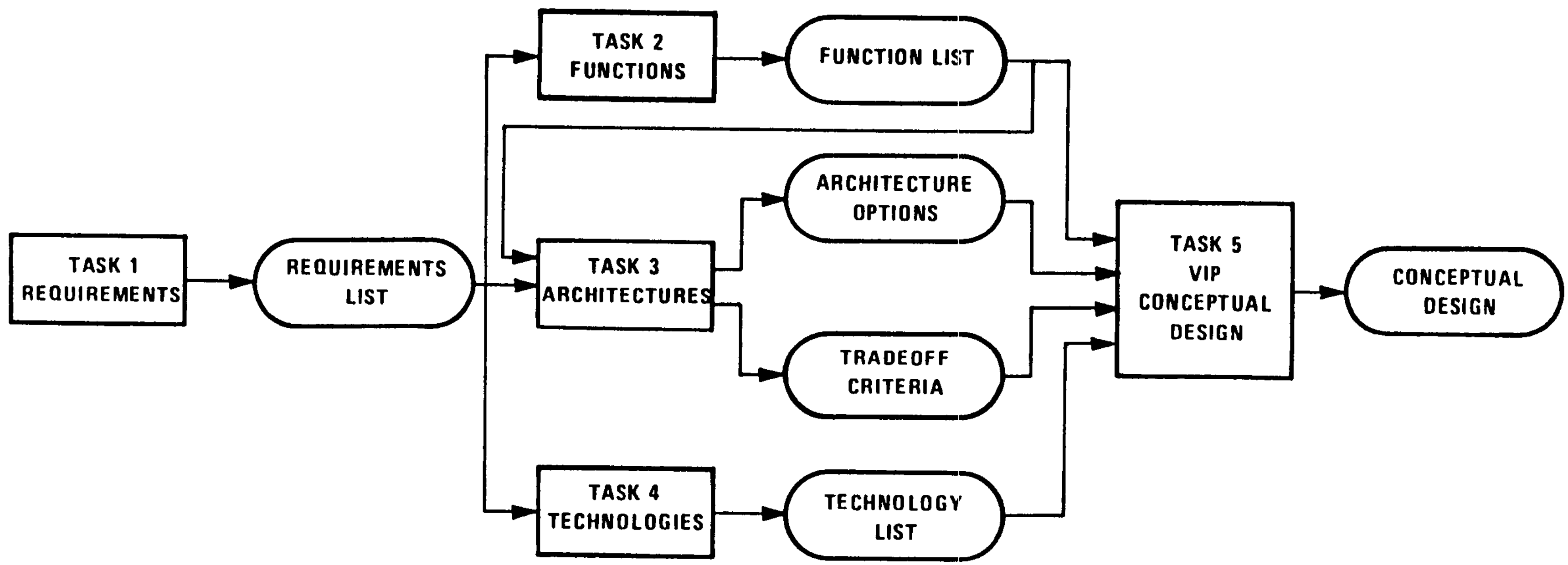
506-58-13/N. D. MURRAY

OBJECTIVE

- RESEARCH AND DEVELOP THE REAL-TIME DATA AND INFORMATION PROCESSING OF VIDEO IMAGE DATA FOR SPACE STATION REQUIREMENTS.

APPROACH

- INVESTIGATE POTENTIAL FUNCTIONS FOR VIDEO RATE IMAGE/VISION SPECIAL PURPOSE PROCESSING, IDENTIFY ARCHITECTURAL APPROACH, AND GENERATE A CONCEPTUAL DESIGN. HONEYWELL
- RESEARCH COMPUTATIONALLY SIMPLE ALGORITHMS AND DETERMINE THEIR IMAGE/VISION EFFECTIVENESS.
- IMPLEMENT SELECTED ALGORITHMS IN SPECIAL HARDWARE DESIGNS AND EVALUATE.
- USING RESULTS OF PROCEEDING EFFORTS, IMPLEMENT AN OVERALL ARCHITECTURAL DESIGN THAT WILL PROVIDE IMAGE/VISION PROCESSING AT VIDEO RATES THAT ARE FLEXIBLE, SELECTABLE AND PROGRAMMABLE.


TASK 1
REQUIREMENTS
REQUIREMENTS
LIST
TASK 2
FUNCTIONS
FUNCTION LIST
TASK 3
ARCHITECTURES
ARCHITECTURE
OPTIONS
TRADEOFF
CRITERIA
TASK 4
TECHNOLOGIES
TECHNOLOGY
LIST
TASK 5
VIP
CONCEPTUAL
DESIGN
CONCEPTUAL
DESIGN

VIDEO SOURCES

- CAMERAS

  INTERNAL

  - MODULE CAMERAS
  - EXPERIMENT MONITORING

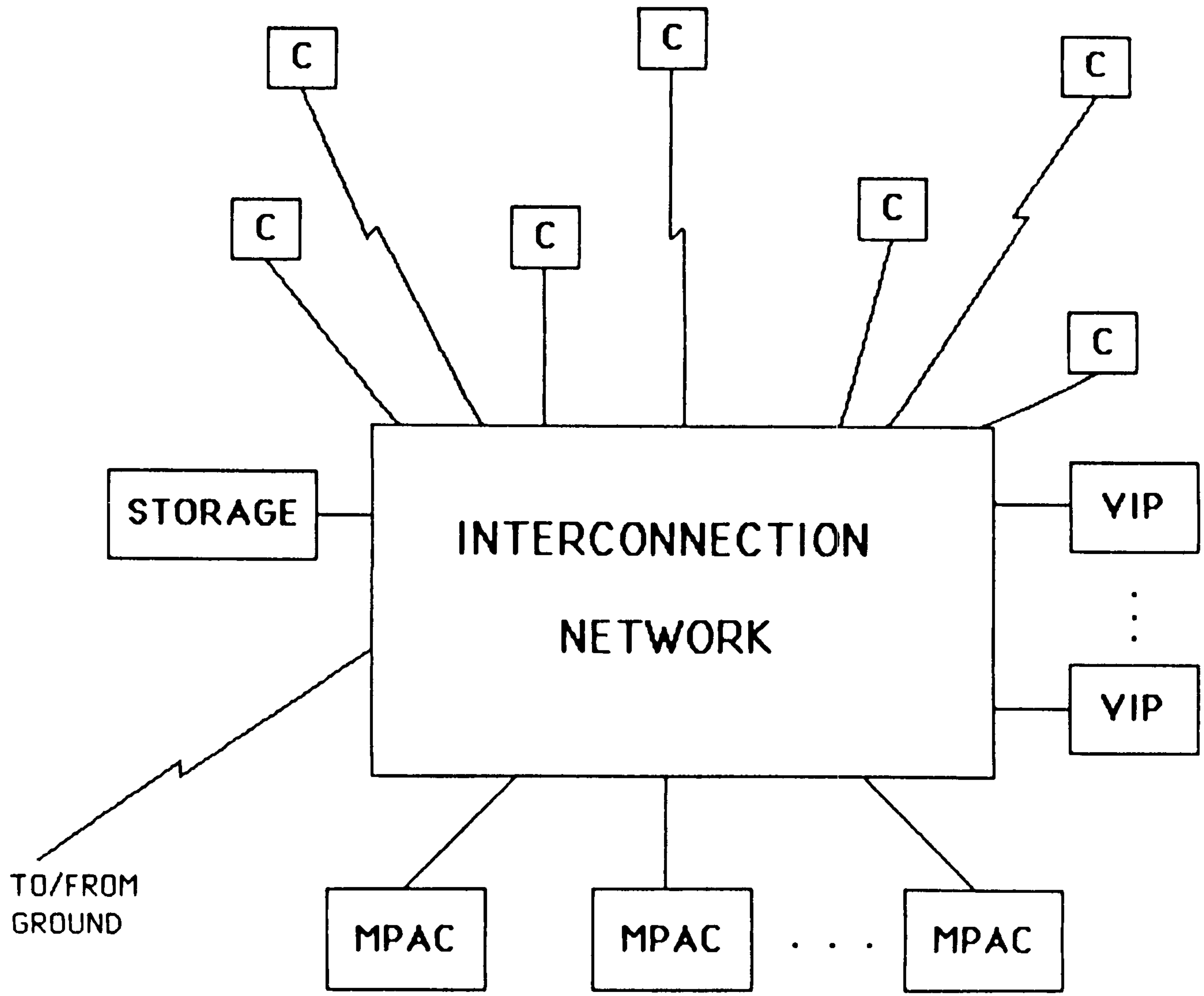
  EXTERNAL

  - MRMS
  - DOCKING PORTS
  - LOCAL AREA TRAFFIC MONITORING
  - SERVICING FACILITY
  - ON MMUS
  - OMV/OTV
  - FREE FLIERS

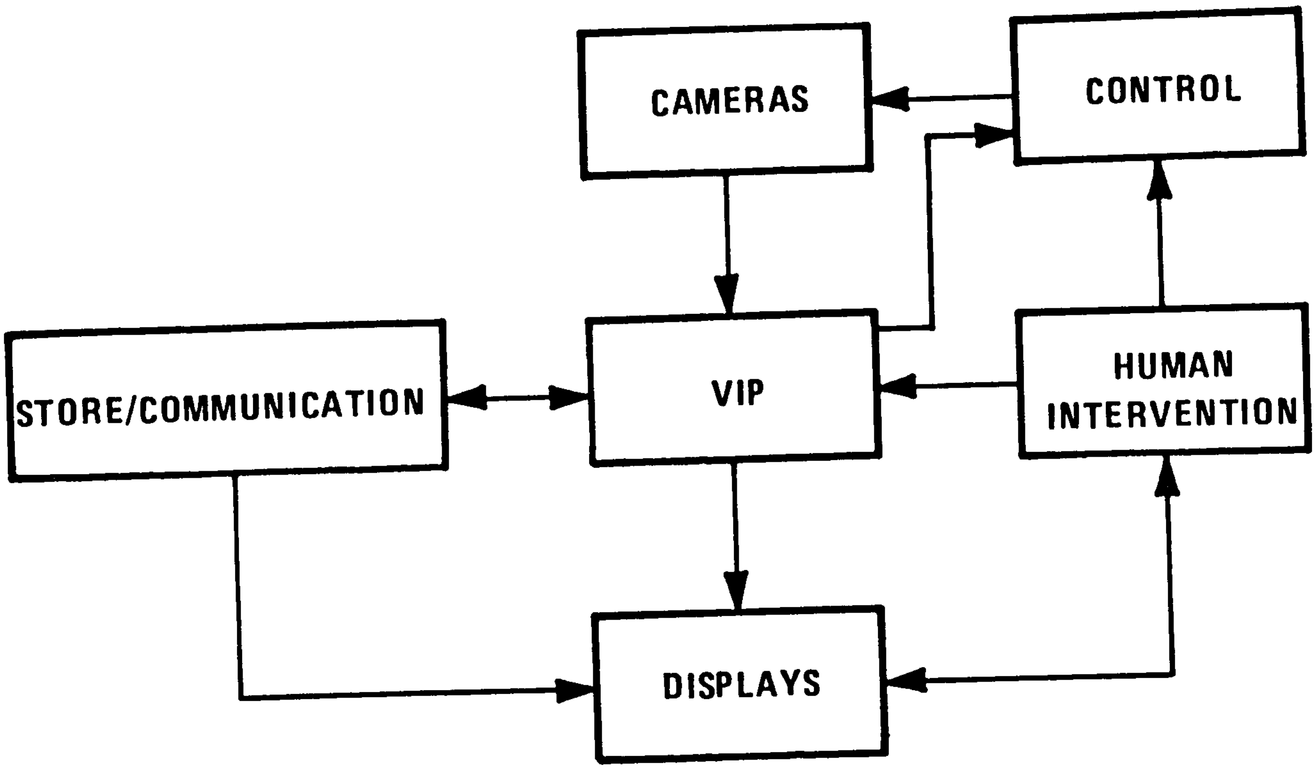
- VIDEO STORAGE DEVICES

- UPLINK VIDEO

VIDEO DISTRIBUTION

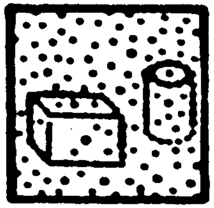


VIDEO IMAGE PROCESSING IN SPACE STATION

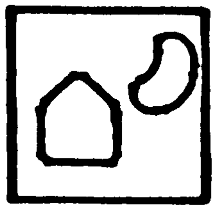


- REAL TIME, 100 MBPS

ALGORITHMS

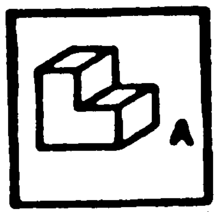


- PROCESSING
  - REMOVAL OF NOISE
  - HISTOGRAM
  - THRESHOLDING

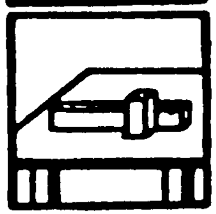


- ANALYSIS

<u>STRUCTURAL</u>	<u>STATISTICAL</u>
EDGES	DENSITY FUNCTION
VERTICES	MOMENTS
REGIONS	CO-OCCURENCE
	MATRICES



- RECOGNITION
  - OBJECTS
  - TEXTURES



- UNDERSTANDING
  - SCENE DESCRIPTION
  - SPATIAL RELATIONSHIP
  - MOTION PARAMETERS

NATURE OF PROCESSING

IMAGE:

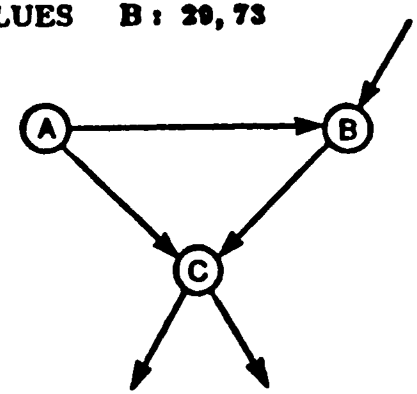
ORDERED SETS OF NUMBERS — 32 64 41 40

IMAGE FEATURES:

SYMBOLS ASSOCIATED WITH NUMERICAL VALUES — A : 37, 26 / B : 20, 73

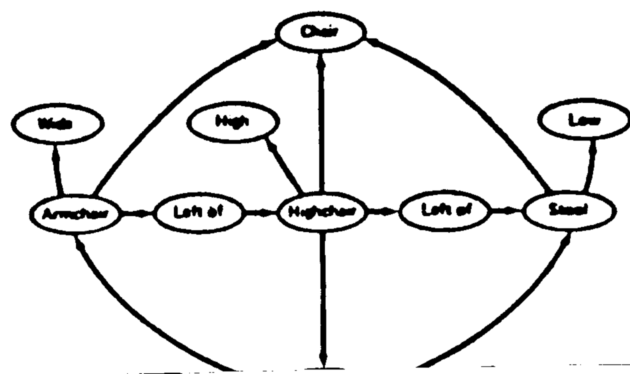
OBJECTS:

INTERRELATED SYMBOLS (GRAPH)



SCENE:

SEMANTIC NETS



FUNCTIONAL ANALYSIS

GOAL: FUNCTIONAL DECOMPOSITION OF SPACE STATION TASKS AND DETERMINATION OF COMPUTATIONAL REQUIREMENTS

FEATURES:

- OPERATION THROUGHPUT
- DATA THROUGHPUT
- POTENTIAL PARALLELISM
- DATA DEPENDENT BEHAVIOR
- WORD SIZE REQUIREMENTS
- OPERATION DENSITY, (OPS/PIXEL OR OPS/FEATURE)
- IMPLICATIONS FOR
  - PROCESSING SUPPORT
  - COMMUNICATION REQUIREMENTS
  - CONTROL STRATEGIES

IMAGE ANALYSIS COMPUTATIONAL MODEL

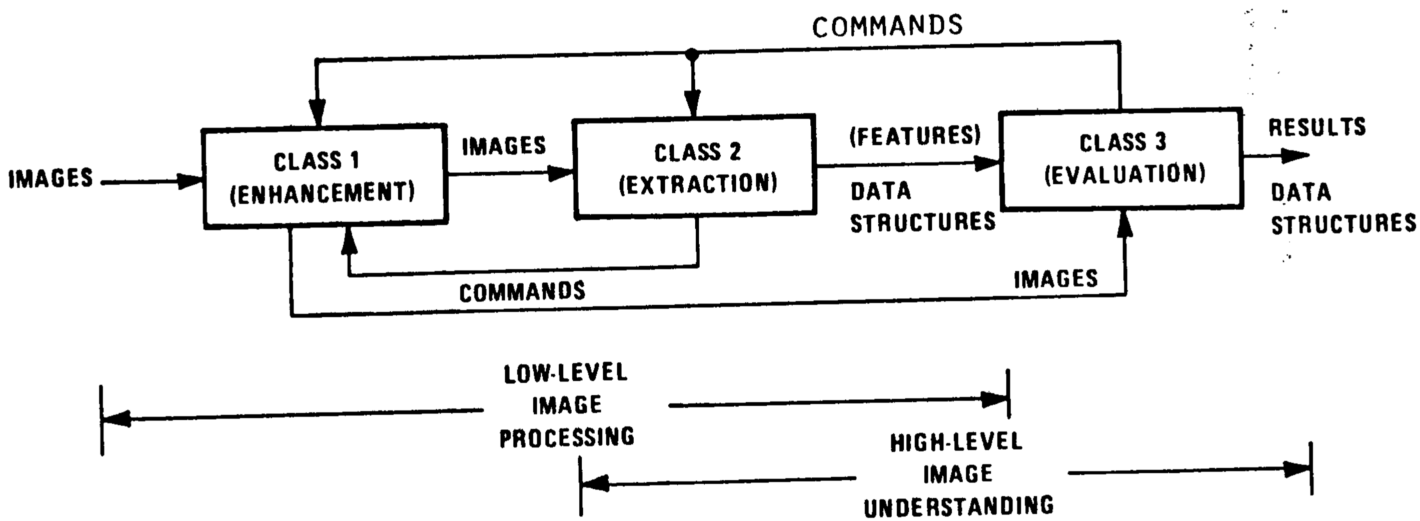


IMAGE PROCESSING ENVIRONMENT

PARALLEL TASKS MAY BE FORMULATED BY EXPLOITING PARALLELISM IN THE TRANSFORMATIONS OR DATA STRUCTURES

TRANSFORMATIONS MAY BE CLASSIFIED AS

- IMAGE TO IMAGE (PREPROCESSING)
- IMAGE TO DATA STRUCTURE (DATA REDUCTION)
- DATA STRUCTURE TO DATA STRUCTURE (HIGH LEVEL)

IMAGE-TO-IMAGE FUNCTIONS

EXAMPLE	MOPS	DATA ACCESS PATTERN
• DETECTOR COMPENSATION	8-9	FIXED, HIGHLY PARALLEL
• THRESHOLDING	8	
• FILTERING	400	
• CORRELATION	400	
• EDGE DETECTION	400-800	
• ENHANCEMENT	100	
• CHANGE DETECTION	8	

IMAGE-TO-IMAGE FUNCTIONS (CONTINUED)

- DATA DEPENDENCIES - VERY LOW
- WORD SIZE REQUIREMENTS - PIXEL RESOLUTION
- OPERATION DENSITY - $10\text{-}10^2$ OPS/PIXEL
- PROCESSING SUPPORT - SIMPLE ARITHMETIC OPERATIONS
- COMMUNICATION - FIXED, PREDETERMINED
- CONTROL STRATEGIES - SYNCHRONOUS, SIMD

IMAGE-TO-DATA STRUCTURE FUNCTIONS

EXAMPLES	MOPS	DATA ACCESS PATTERN
• REGION GROWING	20-30 (EMPIRICAL)	CONSTRAINED
• LINE AND SHAPE DETECTION (HOUGH TRANSFORM)	200-300	FIXED
• ENCODING VIA - QUAD TREES - RECTANGLE CODES	?	?
• STATISTICS	30	PREDETERMINED

IMAGE-TO-DATA STRUCTURE FUNCTIONS
(CONTINUED)

- DATA DEPENDENCIES - TENDS TO BE HIGH
- WORD SIZE REQUIREMENTS - 16 BITS
- OPERATION DENSITY - $10\text{-}10^3$ OPS/FEATURE
- PROCESSING SUPPORT - ARITHMETIC, SOME LOGICAL, LIMITED FLOATING POINT
- COMMUNICATION - CAN BE STRUCTURED IN A MANNER THAT CAN BE PREDETERMINED
- CONTROL STRATEGIES - INCLINED TOWARD MIMD

DATA STRUCTURE-TO-DATA STRUCTURE FUNCTIONS

EXAMPLES	MOPS	DATE ACCESS PATTERN
• MATCHING DESCRIPTIONS		
- GRAPHS	1-3	PREDETERMINED
- CONTOURS	20-30	PREDETERMINED
• MATCHING FEATURE VECTORS	1-2	FIXED
• 3-D STRUCTURE	?	UNKNOWN
• INFERENCE RULE EVALUATION	?	UNKNOWN
• POSITION ESTIMATION, TRACKING	?	UNKNOWN

DATA STRUCTURE-TO-DATA STRUCTURE FUNCTIONS (CONTINUED)

- DATA DEPENDENCIES - VERY HIGH
- WORD SIZE REQUIREMENTS - 32-64 BITS
- OPERATION DENSITY - 10^4-10^6 OPS/FEATURE
- PROCESSING SUPPORT - SYMBOLIC OPERATIONS, DATA MANIPULATION, NON-NUMERIC OPERATIONS
- COMMUNICATION - DYNAMIC, VARIABLE
- CONTROL STRATEGIES - MIMD

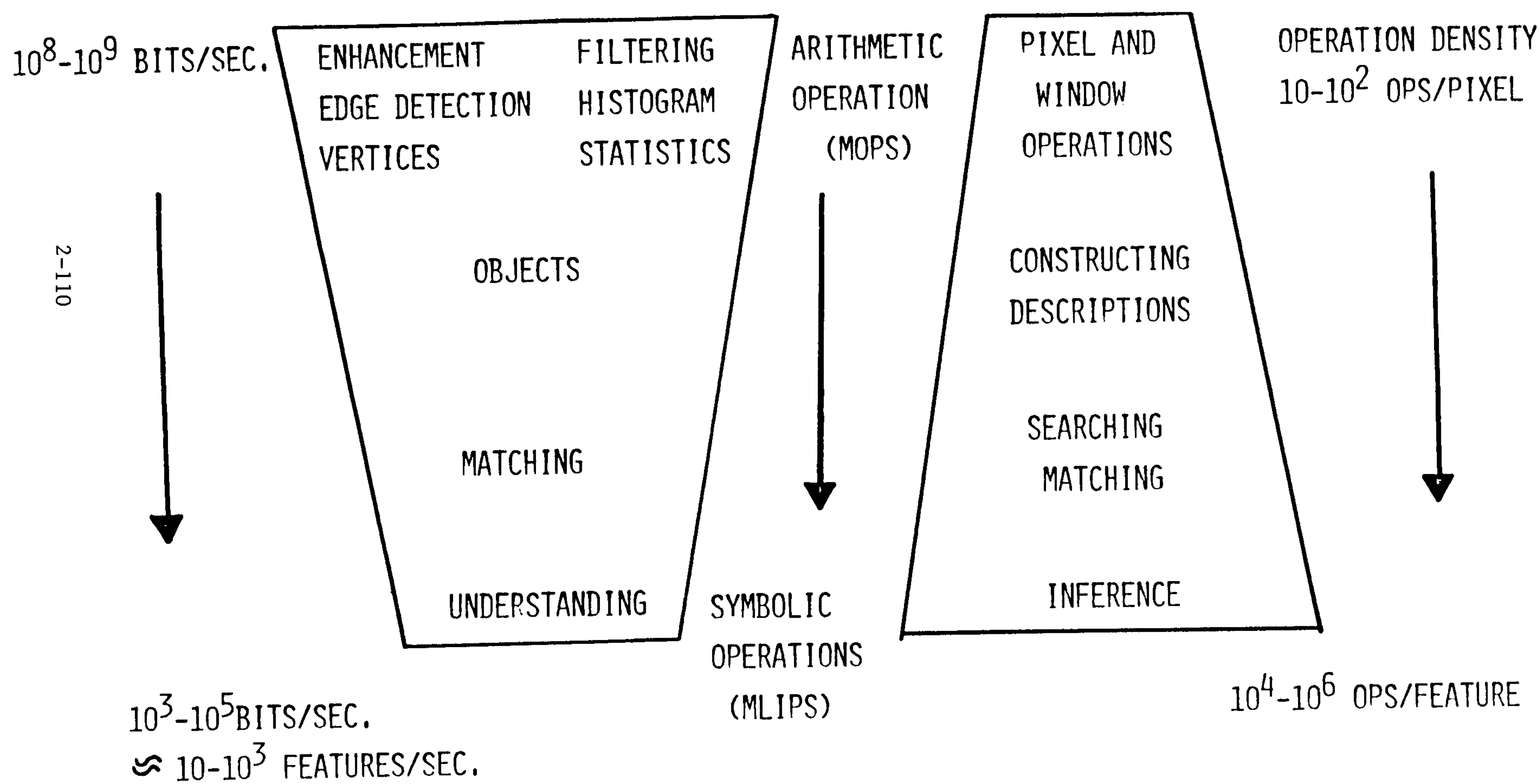
FUNCTIONAL ANALYSIS SUMMARY

	IMAGE TO IMAGE	IMAGE TO DATA STRUCTURE	DATA STRUCTURE TO DATA STRUCTURE
• DATA DEPENDENCIES	LOW	MEDIUM	HIGH
• ACCURACY	PIXEL RESOLUTION	16 BITS	32-64 BITS
• OPERATION DENSITY	$10-10^2$ OPS/PIXEL	$10-10^3$ OPS/FEATURE	10^4-10^6 OPS/FEATURE
• DATA THROUGHPUT	8-500 MOPS	10-300 MOPS	1-5 MOPS, MLIPS
• PROCESSING REQUIRED	ARITHMETIC, SIMPLE	ARITHMETIC, LOGICAL	FLOATING POINT SYMBOLIC NON-NUMERIC
• CONTROL	SYNCHRONOUS (SIMD)	TOWARD MIMD	ASYNCHRONOUS, MIMD
• COMMUNICATION	FIXED	CAN BE STRUCTURED AND PREDETERMINED	DYNAMIC AND VARIABLE

FUNCTIONAL ANALYSIS SUMMARY
(CONTINUED)

- MIX OF COMPUTATIONS AND CONTROL STRATEGIES
- INCREASING NON-DETERMINISTIC BEHAVIOR
- SHIFT IN POTENTIAL PARALLELISM FROM DATA TO ALGORITHMS
- PERHAPS CONFLICTING ARCHITECTURAL SOLUTIONS?
- ROLE OF COLOR NEEDS TO BE DETERMINED
- IMPACT OF DYNAMIC AND STATIC NATURE OF DATA STRUCTURES TO BE EVALUATED

COMPUTATIONAL CHARACTERISTICS



CONCURRENT PROCESSING ARCHITECTURES

- SPECIAL-PURPOSE PROCESSORS
- WORD-SEQUENTIAL PROCESSORS
- ASSOCIATIVE PROCESSORS
- ARRAY PROCESSORS
- PIPELINE PROCESSORS
- RECONFIGURABLE PROCESSORS
- MULTIPROCESSORS
- DATA FLOW PROCESSORS
- OBJECT-ORIENTED PROCESSORS
- INFERENCE PROCESSORS

p. 13

FIBER OPTICS WAVELENGTH DIVISION MULTIPLEXING (COMPONENTS)

HERBERT D. HENDRICKS

NASA LANGLEY RESEARCH CENTER

Long Term Objectives:	Develop optical multiplexers/demultiplexers, different wavelength and modulation stable semiconductor lasers, high data rate transceivers and test and evaluate in fiber optic networks applicable to Space Station
Importance of Problem:	Information networks for space data systems require high data rate and high data capacity which can be expandable and fault tolerant. Fiber optics wavelength division multiplexing provides all of these options through the multiplicity of wavelengths available.

FIBER OPTICS WAVELENGTH DIVISION MULTIPLEXING (COMPONENTS)

Herbert D. Hendricks
NASA Langley Research Center

Related R & D: Comments related to other R & D in this area has been obtained from AGED "C" reviews, Tri-Service Working Group on Fiber Optics, Published Literature and Private Communications.

Optical Multiplexer/ Demultiplexer Technology: DOD/RADC through contract to ITT has demonstrated a twelve channel point to point mux/demux with an insertion loss of 8 dB and a cross talk of 17 dB. LaRC evaluated device for RADC independently of contractor. Current status-design being improved. This device works in 1.3 micrometer region and has 15 nanometer spacing between channels.

Boeing/Martin Marietta have laboratory experiments with six channel mux/demux systems. PTR supplied device to Boeing with approximately 5 dB insertion loss and cross talk in 15 dB range and a channel spacing of 20 nanometers. JDS (Canadian Co.) supplied Martin Marietta with a six channel device with a 2.5 db insertion , approximately 20 dB crosstalk and 25 nanometer channel spacing. All channels in 1.3 micrometer region.

FIBER OPTICS WAVELENGTH DIVISION MULTIPLEXING (COMPONENTS)

Herbert D. Hendricks
NASA Langley Research Center

Related Technology:

Optical Multiplexer/Demultiplexer Technology:

BTL performed a "hero" demonstration of a point to point 10 channel system operating at 2 nanometer channel spacing (possibly 20-30 dB cross talk), no insertion loss given, while operating the data system at 2 GBits. System used 1.5 micrometer DFB semiconductor lasers.

Instruments S.A. (Metuchen, NJ), a subsidary of a French company(Jovin), reported a 49 channel device at the SPIE(8/85) in San Diego. Discussions with the author revealed a device cross talk of 15 dB, channel spacing of 1.2 nanometer but only with a matched mux/demux pair in point to point data systems. Data Rate was 50 kBits in the 0.8 micrometer region of the spectrum.

Quante Corporation used a NEC filter type mux/demux with 3-4 dB insertion loss and 15 dB cross talk in a four wavelength system in 0.8 micrometer region of the spectra. Channel spacing was 30 nanometers. Quante also announced a system in the 1.3 micrometer region using single mode fibers. The original work was done for the German post-office.

FIBER OPTICS WAVELENGTH DIVISION MULTIPLEXING (COMPONENTS)

Related Technology:	
Semiconductor Lasers:	Distributed Feedback Semiconductor Laser Technology has mainly centered around R & D in Japan and BTL in terms of demonstration of utility. Modulation rates up to 4 GBits were demonstrated in the laboratory with a 1.5 micrometer device by BTL. Japanese accomplishnments have been just as significant with an addition plus of a demonstrated lifetime of at least 10,000 hours without any wavelength shift. Current R & D is being funded at RCA by NASA for Ridge Guide Device in the 1.3 & 1.5 micrometer region of the spectra. DOD has funded a SBIR effort with General Optronics but no device announced.
Other Semi-Conductor Lasers:	RCA, General Optronics, Lasertron, & Laser Diode Laboratory are the main known suppliers of different wavelength lasers in the 0.8, 1.3 & 1.5 micrometer region. GTE, Ortel and Spectra Diode Labs. have been involved to a lesser extent. Twelve different wavelengths have been the maximum number supplied in any one wavelength region to date.

Related Technology:

Transceivers: The DOD has a number of military qualified transceivers demonstrated up through 50 Mbits. Current RADC/NASA activity is addressing devices Military/Space qualified up through 200 MBits and available within a year. Transceivers are being breadboarded with military qualified components up through 1 GBit (NASA/RADC).

Commerical transceivers are available in various configurations and wavelength regions up to the 500-700 Mbit/sec(NRZ) range. BTL is planning on installing 1728 MBit transceivers/systems begin-ing in 1986.

DARPA is funding monolithic transceiver technology in GaAs material system with Honeywell and R. I. The Japanese have reported a number of integrated transmitter and receiver front ends(i.e. the integration of a laser or photodetector with a GaAs FET technology.

At least four companies offer foundry services for high speed front end circuit design for hybrid systems which is currently the most advanced and practical intermediate system.

FIBER OPTICS WAVELENGTH DIVISION MULTIPLEXING (COMPONENTS)

Related Technology:

Fiber Optics Networks: Many point to point WDM systems have been demonstrated. Greatest number has been 12 by ITT in a RADC demonstration contract. Data rate only 40 MBits and no BER data(1.3 micrometer spectral region). Quante has a four channel point to point WDM data system running at 140 MBits (A commerical system). BTL demonstrated in the lab. the highest data rate, 4 MBits, in a 10 channel point to point single receiver set up.

A number of companies are looking at the "Star" bus approach but mainly in the labs. Noteably Harris, Martin Marietta, Lockheed and Boeing

Many companies have studies of the WDM technology looking at network approaches. Noteably GTE, Honeywell, Xerox, Mitre, RCA, TRW, ITT, etc.

FIBER OPTICS WAVELENGTH DIVSIION MULTIPLEXING (COMPONENTS)

Technical Approach:	The technical approach has been a many faceted approach drawing from a combination of contract, military efforts, in-house and demonstration and application of the component technology.
Mux/Demux:	A combination of contracts for grating demux technology, direct procurements of best effort prism gratings, in-house interference filter demultiplexer design and participation in and evaluation of RADC & ERADCOM contract designs. Assessment of advances of technology from available literature and published reports. Objectives of all of the approaches has been to reduce the device insertion loss, decrease the optical spacing between channels and improving the cross talk isolation.
Semiconductor Laser:	A combination of contractural efforts, coordination with DOD efforts, and evaluation of contracturally developed devices and commerically available devices. Published literature and conference reported advances serve to assess progress and limitation. Insertion of devices into actual prototype applications also serves as a method of determining and assessing device properties and specific utility.

FIBER OPTICS WAVELENGTH DIVISION MULTIPLEXING (COMPONENTS)

Technical Approach:

Transceivers: Active transmitter and receiver designs have been a regular in-house activity to implement a variety of demonstration data networks. Coordination of work in this area has been with the Tri-Service Committee on fiber optics and industrial sources which have advanced the state of the art. Joint efforts have been with RADC to supplement NASA programs in this area.

Fiber Optics Networks: Components have been built into a variety of networks ranging from point to point, star and mesh types to demonstrate the performance of the devices. A central theme has been maintained in demonstration of the networks. That theme is to utilize the passive coupling nature of fiber optics and eliminate the need for repeaters. The idea of modularity and repeatibility of the network configuration with gateway type communications has also been implemented. Numerous discussions on the methodology to implement the technology have been held with DOD, industry, universities and NASA researchers.

FIBER OPTICS WAVELENGTH DIVISION MULTIPLEXING (COMPONENTS)

Technical Results and Accomplishments

Multiplexer/Demultiplexer Technology

Tested and evaluated three prism grating demulti-designs, one Rowland Grating design and one Littrow Grating design(RADC/ITT).

Semiconductor Lasers

Continued in-house evaluation and insertion program in transmitter design. Funded InGaAsP DFB laser development in 506 58 23 area.

Transceivers

Demonstrated in-house designed fiber optic transceiver operating at 500 MBits. Designed 0.5-2 GBit front end transceiver based on GaAs FET technology. Implemented 200 MBit transceiver program with RADC to develop military/space qualified version. Implemented 1 GBit military qualified bread board design program.(482 58 13)

FIBER OPTICS WAVELENGTH DIVISION MULTIPLEXING (COMPONENTS)

Technical Results and Accomplishments

Fiber Optics WDM Networks

Demonstrated components in an 8 channel star bus configuration using 810, 820, 830, 840, 1250, 1300, 1350 and 1500 nanometer wavelengths.

Achieved less than 10^{-10} bit error rate in 8 channel star bus with 0.8 and 1.3 micrometer wavelength system operating at 20 MBits and 500 MBits.

Demonstrated 32 node multi-mode fiber optics network operating at 500 MBits worse case condition with 10 dB excess dynamic range.

Designed 60 node single mode fiber optics mesh network based on 3 x 3 star couplers.

Initalized network within a network using WDM.

Progress towards planned milestones have exceeded estimations.

FIBER OPTICS WAVELENGTH DIVISION MULTIPLEXING (COMPONENTS)

HOW CURRENT RESULTS AND ACCOMPLISHMENTS WILL ENHANCE NASA CAPABILITY IN COMPUTER SCIENCE AND DATA SYSTEMS.

Current results demonstrate the WDM concept. Through its implementation more parallel channels of data can be transported with less interference, at higher data rates, with implementable fault tolerance approaches for self repairing. That networks can operate within networks that have a common physical connection. This thus provides a more powerful parallelism for network inconnection for an expandable and evolutionary data systems approach for Space Station

An example of this technology expansion capability using just 12 wavelengths and the 32 node fully connected star bus can be demonstrated. Twelve(12) mux/demux systems can be connected at each of 32 ports giving 384 transmitter/receiver pairs running at 500 MBits. Reducing data capacity due to some type of time sharing of the 12 individual networks within a network the data rate could easily be a composite total of 6 Gbits/sec. If the 500 MBit transmitter/receivers are electronic multiplexed and demultiplexed at the highest VHSIC data rate reported, 30 MBits, 17 VHSIC microprocessors could be accommodated at each of the 384 transmitter receiver pairs. This would provide an interconnect between6528VHSIC type processors capable of processing6 Gits/secof data.

FIBER OPTICS WAVELENGTH DIVISION MULTIPLEXING (COMPONENTS)

MAJOR MILESTONES

Demonstrate improved demultiplexer design with reduced insertion loss, increased channel spacing and reduced cross talk - 9/85

Continue to demonstrate components in networks both multi-mode and single mode optical fiber systems directed toward 2 MBits-2GBit/sec systems - 9/86

Demonstrate high performance WDM components (2 GBits) -9/86

Demonstrate DFB laser transmitter - 3/87

RESOURCE REQUIREMENTS	85	86	87	88	89
($k)	175	350	450	450	450
(MY)	0.5(2)	1.5(2)	1.5(2)	1.5(2)	1.5(2)

FIBER OPTICS WAVELENGTH DIVISION MULTIPLEXING (COMPONENTS)

Issues: Funding level, Space Station Qualification Requirement, Space Station Systems Requirements

Comments: All programs coordinated with DOD-Tri-Service Committee on fiber optics and AGED Working Group "C"

Publications/Presentations of Record - Invited Talk and invited paper onn WDM, 3 Conference Publications on WDM components/networks

N87-29152

FIBER OPTIC DATA SYSTEMS

R. Hartenstein
NASA Goddard Space Flight Center
April 17, 1985

Abstract

This paper is an overview of a continuing data system architecture development effort that started at GSFC with OAST support approximately three years ago. The paper also provides accomplishments and states of the OAST effort and a brief comment on possible future directions. The Space Station Focused Technology (SSFT) program has picked up support of this effort and that portion will be addressed during the SSFT discussions.

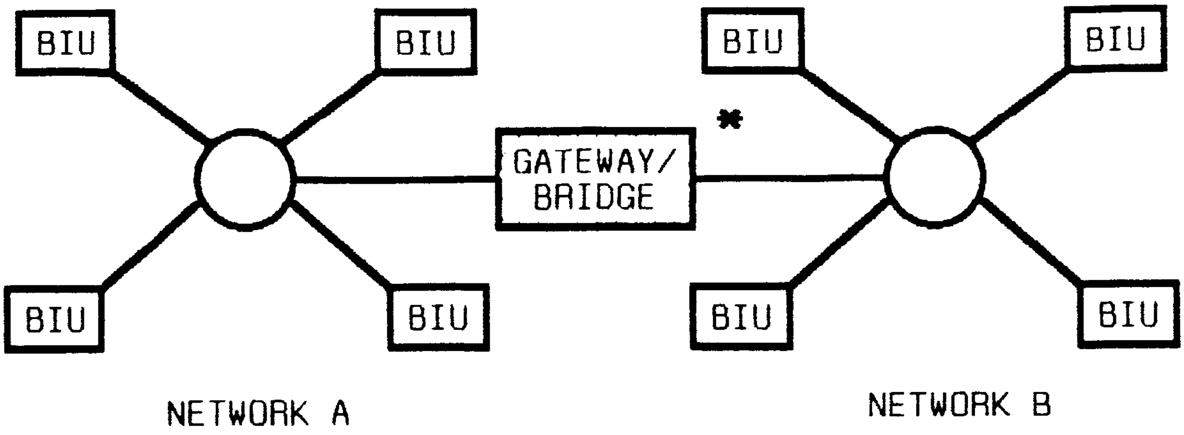
The Star bus was originally chosen for investigation because it seemed to offer unique features unavailable with other topologies. It offered a broadcast mode where everyone received the message at the same time and users could come and go at will without affecting the rest of the system in any way. In order to address the reliability issue, we instituted both a component qualification program and redundancy techniques in the BIU design. The major effort in developing a data network has been the FODS contract at Sperry Flight Systems in Phoenix, Arizona. The FODS (Fiber Optic Demonstration System) consists of a fully redundant Star Network with a 100 megabit signaling frequency. The paper presents some performance data on the access protocol utilized and compares it with other access protocols. The status of the qualification effort is presented showing the successful qualification testing of cables, connectors, and some LEDs and PIN diodes. The point of the future directions charts is that we must begin seriously dealing with multiple topologies and methods for smoothly "growing" them from IOC to the growth systems on Space Station.

GSFC

FIBER OPTIC DATA BUS

TECHNOLOGY

	OAST	SSFT
• STAR BUS TECHNOLOGY	X	
• COMPONENT QUALIFICATION	X	
• NOS/DOS PROTOTYPE		X
• GATEWAY / BRIDGE		X
• VLSI IMPLEMENTATION		X
• FUTURE DIRECTIONS		X

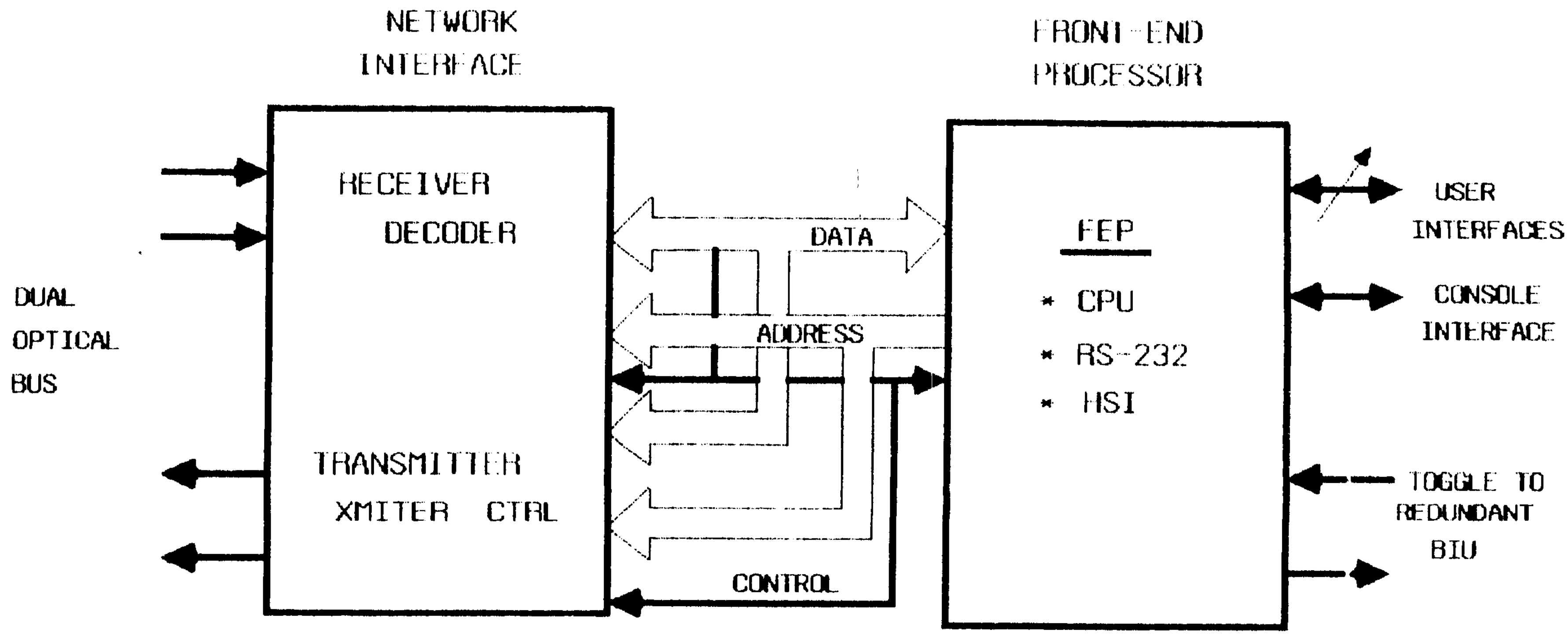


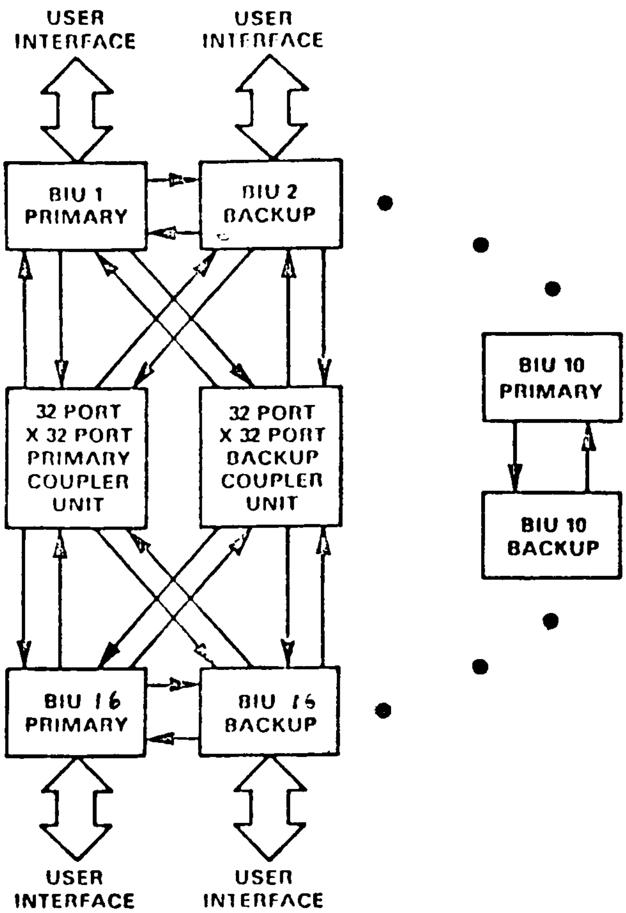
SPERRY FODS

- 100 MB FIBER OPTIC LAN
- 30 MB MAX / BIU
- CSMA / CD / TS OR TS PROTOCOL
- DISTRIBUTED CONTROL
- DUAL PORTED BIU'S

* TO BE DEVELOPED

BIU BLOCK DIAGRAM





FODS REDUNDANT SYSTEM CONFIGURATION

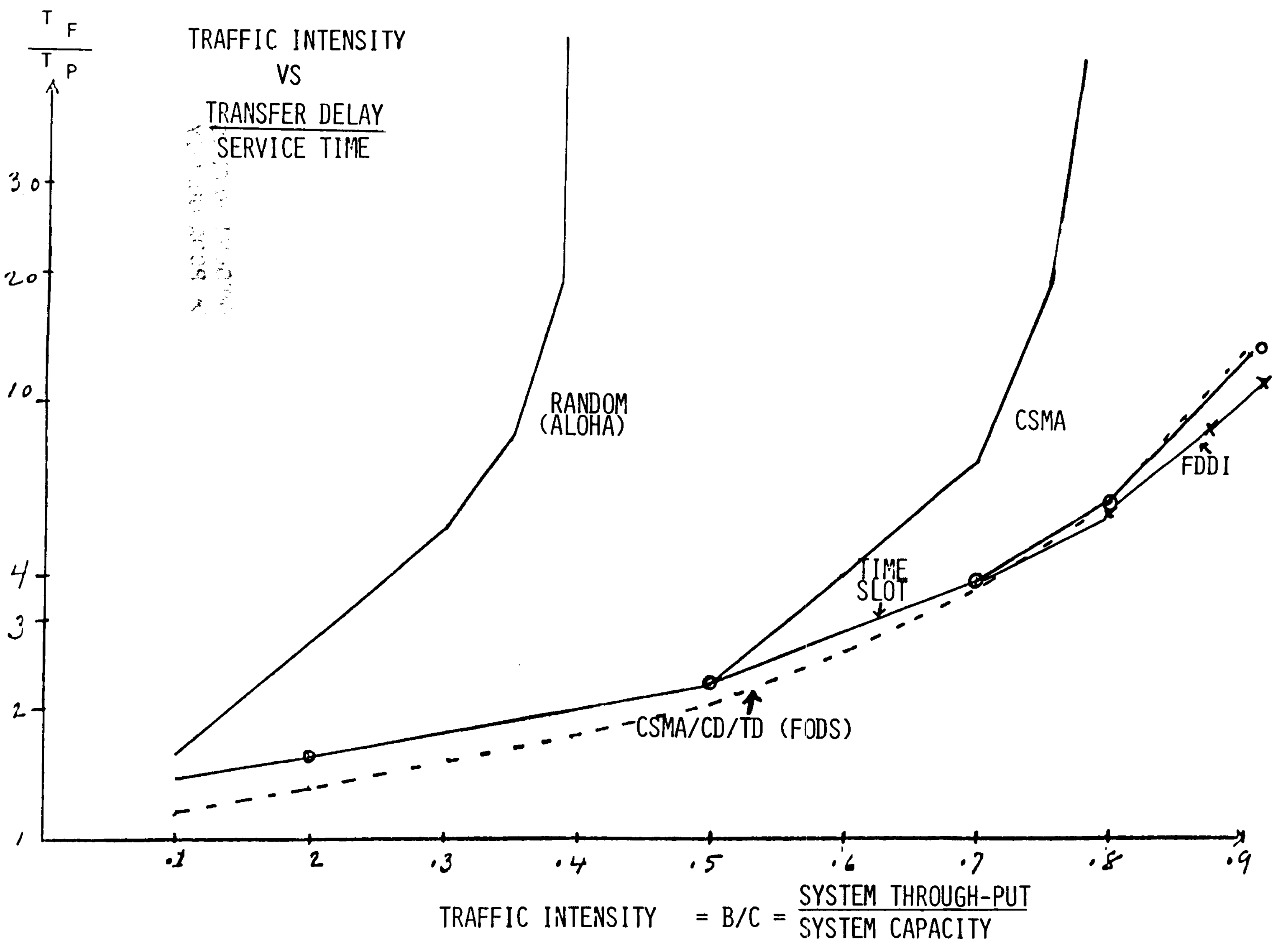


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TABLE I
FODS PARTS QUALIFICATION STATUS

Part #	Part Type	Manufacturer	Test	Results	Status
MFOE 1201	LED/Emitter	Motorola	Qual.	Pass	Report
MFOE 1202	LED/Emitter	Motorola	Screening	----	Test
MFOD 1100	PIN/Detector	Motorola	Qual.	Pass	Report
C30971E*	PIN/Detector	RCA	Analysis	----	Test
SFC-20x20-F*	Coupler	Aetna (ADC)	Evaluation	Pass	Report
OC-1040-10	Cables	Brand Rex	Qual.	Pass	Report
840R	Fiber 200/240	Spectran	Qual.	Pass	Report
200-S	Connector	OFTI	Qual.	Pass	Report
906-122-5003	Connector	Amphenol	Qual.	Pass	Pacer
SFC-32x32-F*	Coupler	ADC	Qual.	----	Procurement

* Further testing required for flight qualification

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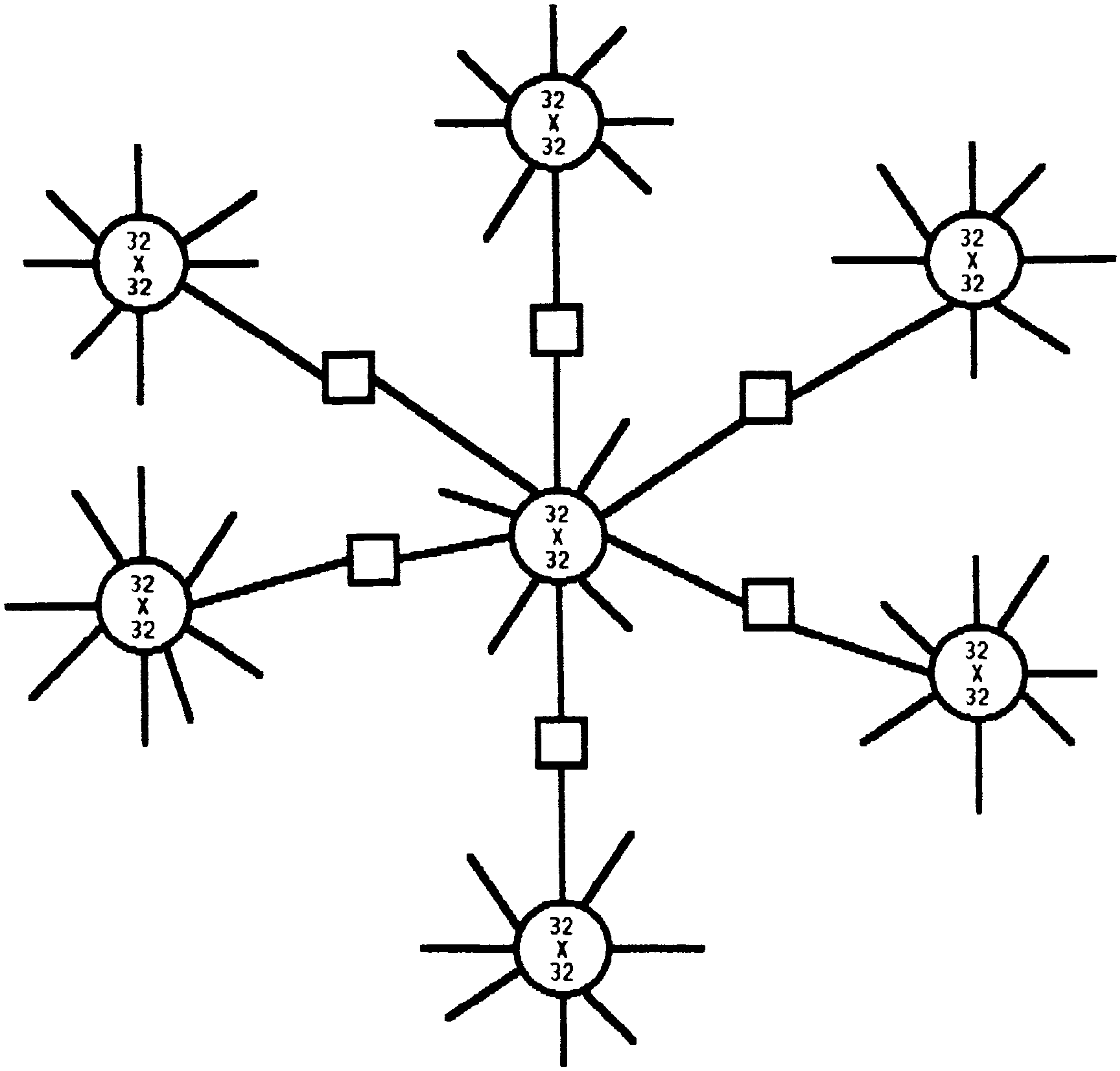
FUTURE DIRECTIONS

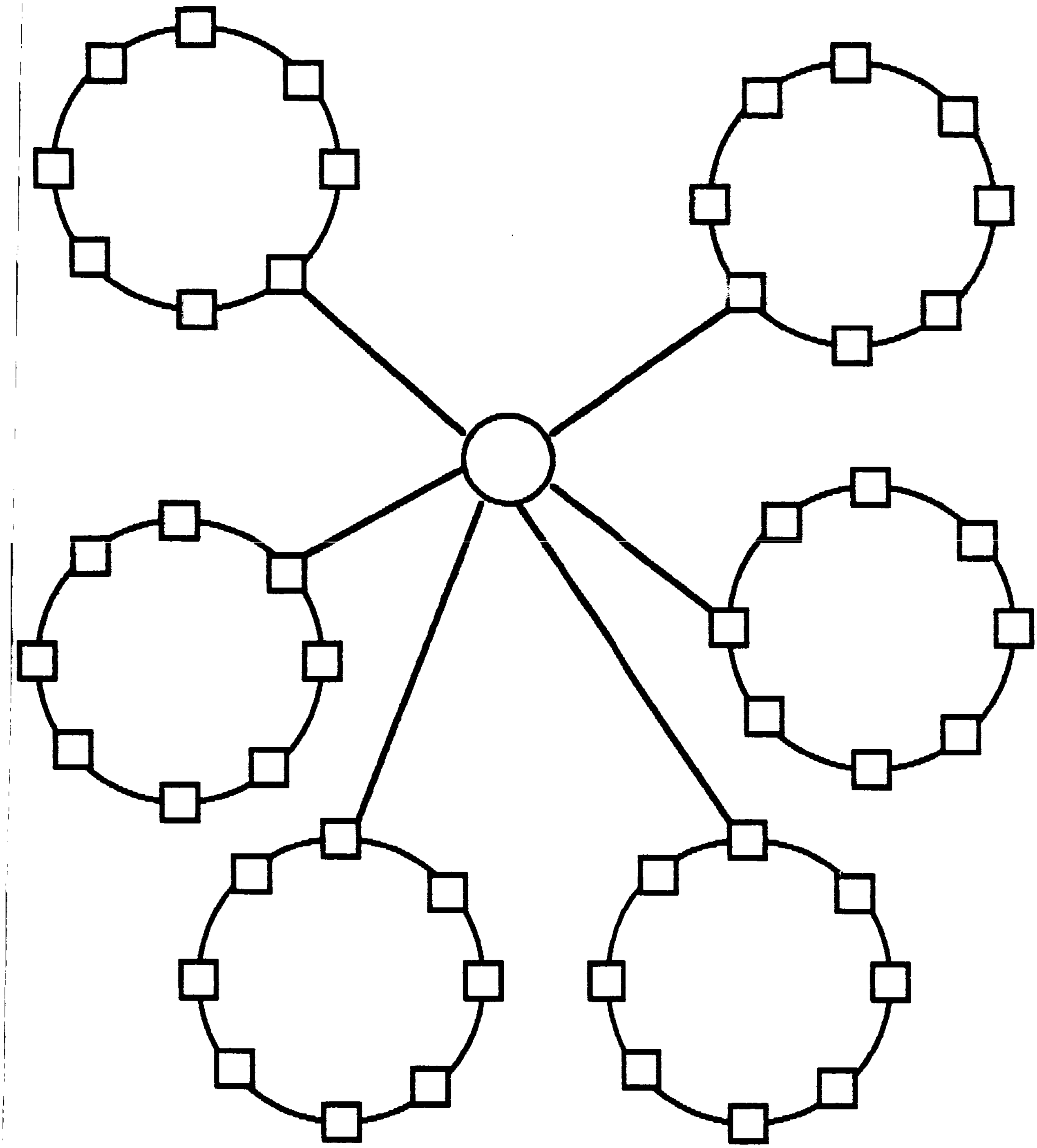
- NEED RELIABILITY
- NEED GROWTH / FLEXIBILITY
- GET AWAY FROM STARBUS

GSFC

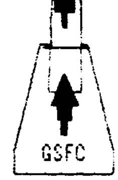


SUPER STAR

- 32 X 32 = 1024 PORTS (992 USER)
- DUAL STARS / BIU's DOUBLE PORTED
- TWO–WAY THRU–WAYS
- TIME DELAYS ALL EQUAL
- TRAFFIC PATTERN SENSITIVE



STAR RING



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ADVANCED LOCAL AREA NETWORK CONCEPTS

This technology development program for onboard Local Area Network (LAN) Concepts is based on a balance of academic studies of new protocol and topology through university grants together with in-house analysis and development of simulation tools. In-house simulation of LAN concepts is being backed up by analytic performance models. Another major element of this program is the constant review of the current outside literature on LAN analysis and the review of the Space Station Data System Architecture Study reports.

Development of a good model of the data traffic requirements for LANs onboard the Space Station is a driving problem in this work. A parameterized workload model is under development with its structure to be circulated for comments to other NASA researchers, the potential user community, and the system development contractors. An analysis contract has been started specifically to capture the distributed processing requirements for the Space Station and then to develop a top level model to simulate how various processing scenarios can handle the workload and what data communication patterns result.

Most of the studies are ongoing and the material presented here should be taken as only a sampling of the work. Attached are three distinct items: (1) a summary of the "Local Area Network Extensible Simulator II Requirements Specification", (2) excerpts from a recent Stanford University grant report by M. M. Nassehi, F. A. Tobagi, and M. E. Marhic, "Topological Design of Fiber Optic Local Area Networks with Application to Expressnet", and (3) as an appendix, from a Santa Clara University grant, Prof. T. J. Healy, "Coding and Decoding for Code Division Multiple User Systems," IEEE Transactions on Communications, April 1985.

ADVANCED LOCAL AREA NETWORK CONCEPTS

TERRY GRANT
NASA-AMES RESEARCH CENTER
APRIL 1985

LOCAL AREA NETWORK EXTENSIBLE SIMULATOR (LANES)

OBJECTIVE: TO PROVIDE A SIMULATION MODELING CAPABILITY OF ONBOARD LOCAL AREA NETWORK (LAN) CONCEPTS WITH APPLICATION TO THE SPACE STATION DATA SYSTEM

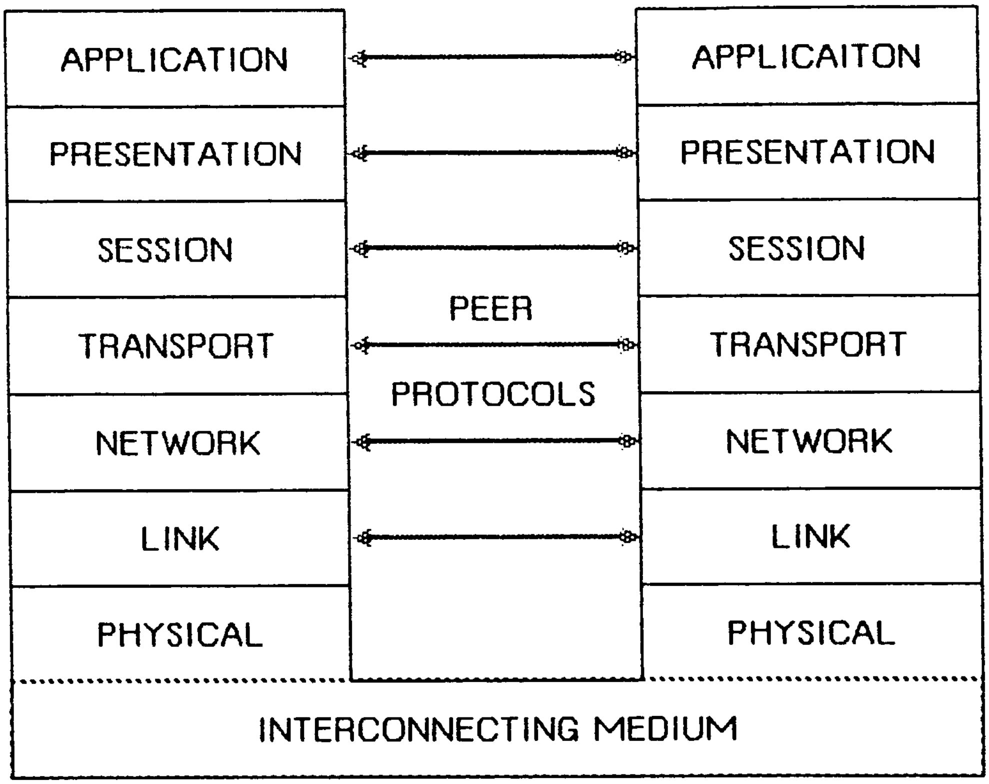
JUSTIFICATION: TO PROVIDE FOR DEVELOPMENT AND TECHNICAL INTERCHANGE OF VIABLE SPACE STATION LAN DATA SYSTEM CONCEPTS THROUGH SIMULATION MODELING

APPROACH: DEVELOP A VERSATILE MODEL OF LAN TECHNOLOGY THROUGH IMPLEMENTATION OF THE ISO-OSI NETWORK PARADIGM USING STATE-OF-THE-ART MEDIA ACCESS RULES AND PHYSICAL LAYER TOPOLOGIES.

TECH TRANSFER: DELIVER SIMULATION CAPABILITY FOR EXPERIMENTATION THROUGH REMOTE ACCESS OF LANES VIA TELENET AS INDIVIDUAL MODELS ARE DEVELOPED:

- NASA CENTERS
- INDUSTRY
- UNIVERSITIES

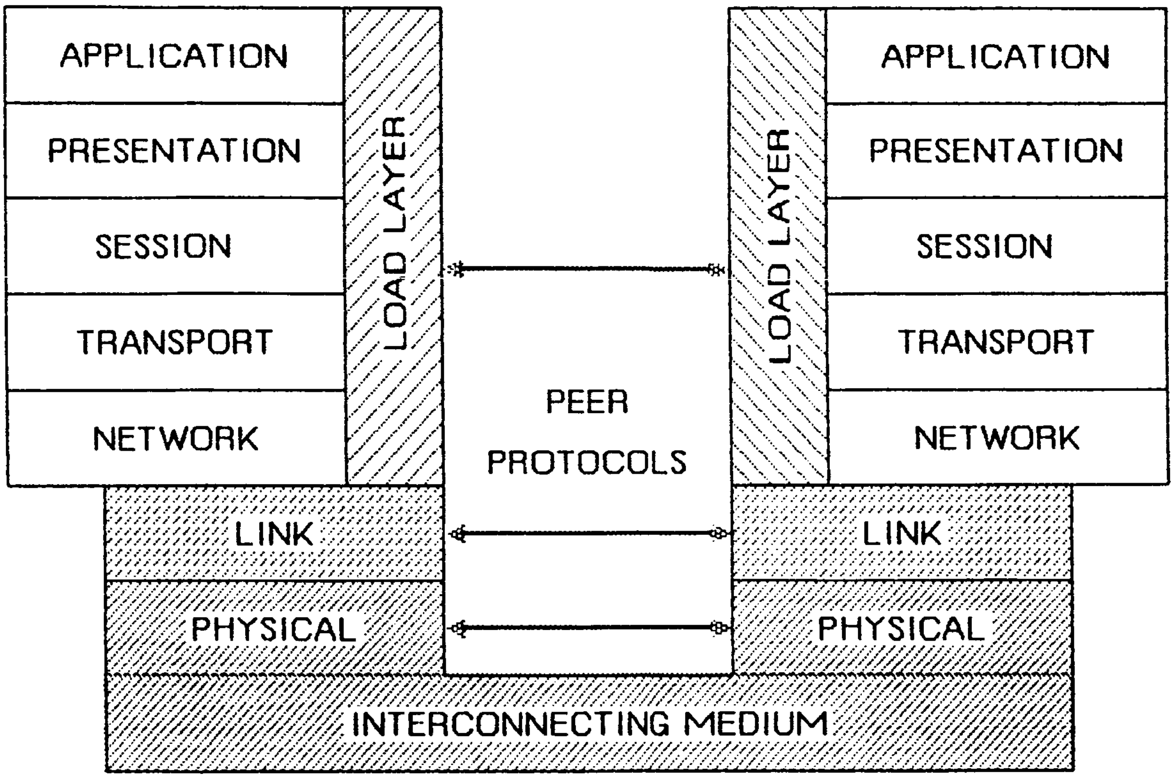
INTERNATIONAL STANDARDS ORGANIZATION—
OPEN SYSTEMS INTERCONNECT
(ISO—OSI)
REFERENCE MODEL



LOCAL AREA NETWORK EXTENSIBLE SIMULATOR

VERSION I

ISO-OSI MODEL



PHYSICAL LAYER - PASSIVE STAR

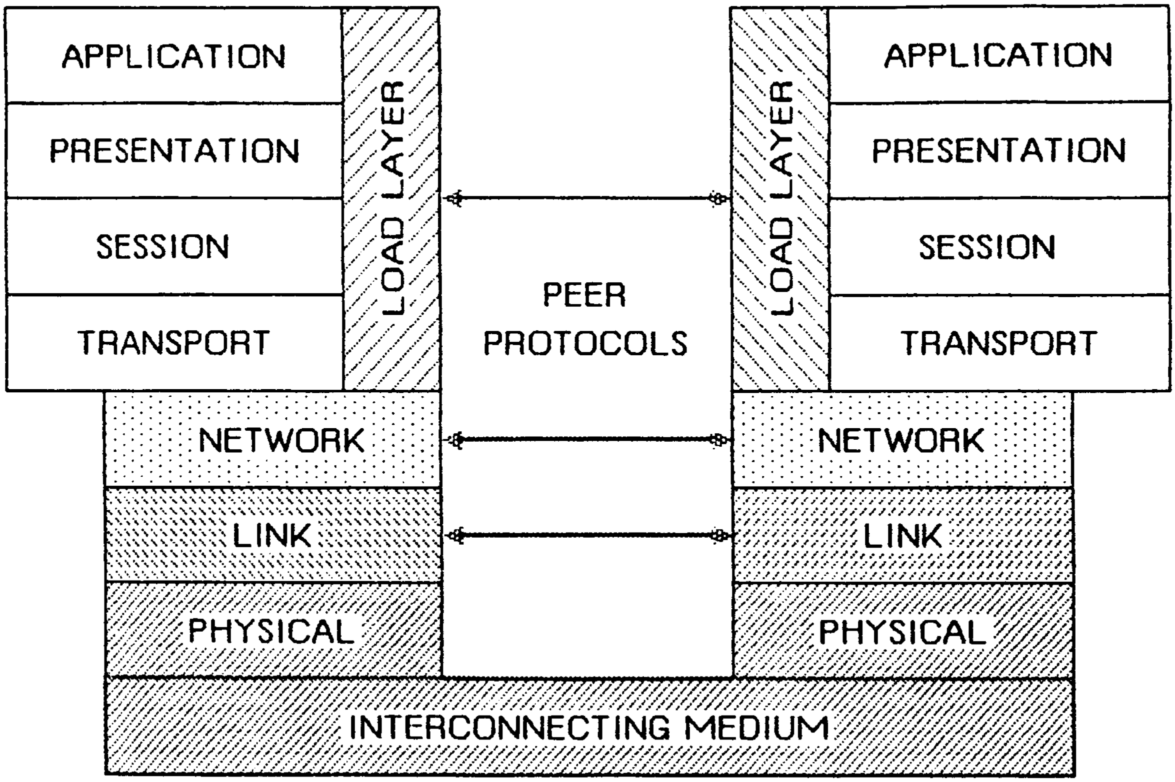
LINK LAYER - CSMA/CD/TS (FODS) PROTOCOL

LOAD LAYER - SINGLE MESSAGE SIZE,
USER DEFINED MESSAGE INTERARRIVAL TIME
USER DEFINED MESSAGE ABSORPTION TIME

LOCAL AREA NETWORK EXTENSIBLE SIMULATOR

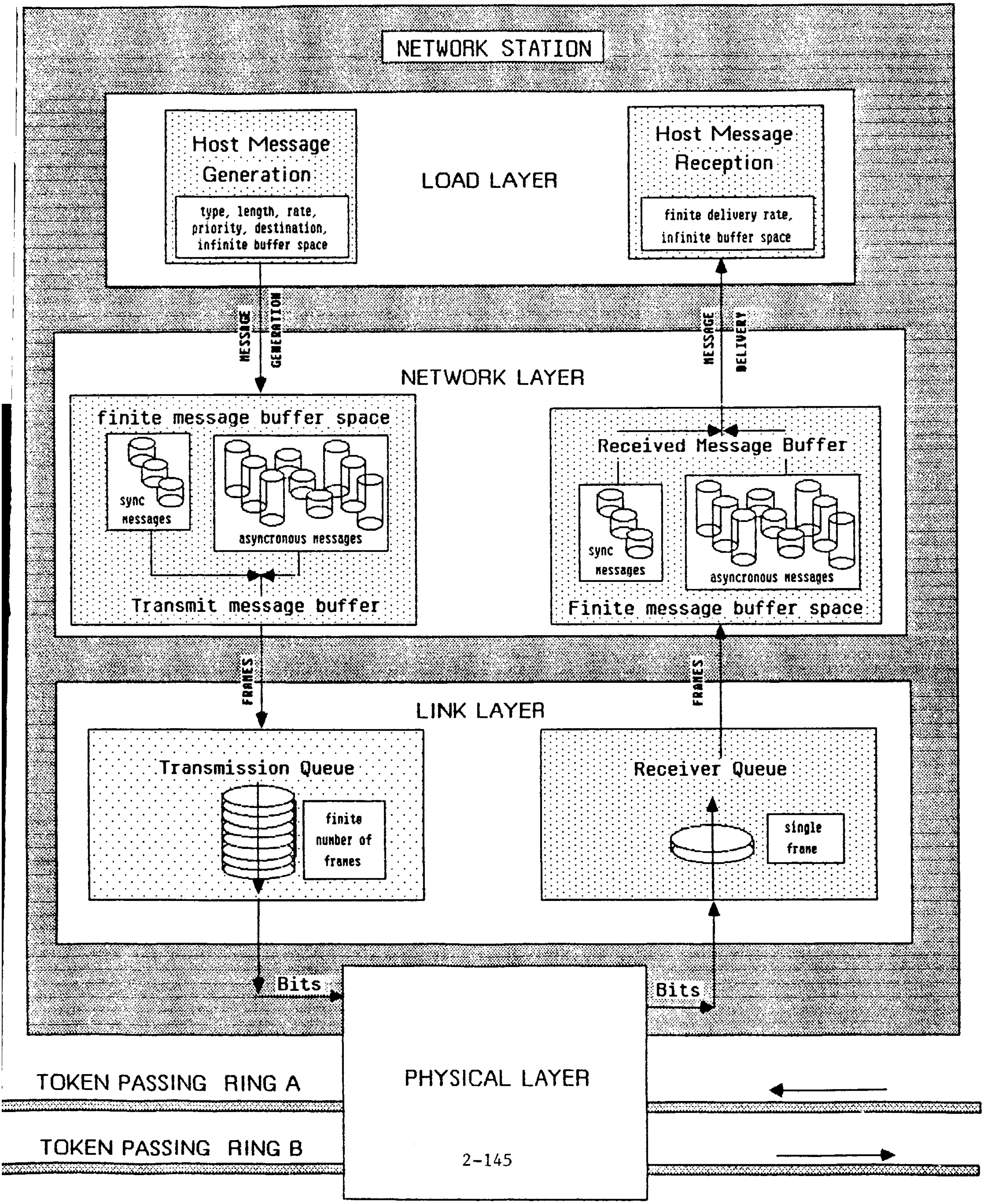
VERSION II

ISO–OSI MODEL



PHYSICAL LAYER	- STAR OR TOKEN PASSING RING
LINK LAYER	- FODS OR FDDI TOKEN RING MEDIA ACCESS CONTROL (ANSI X3T9/84-X3T9.5/883-16 Rev. 7.2)
NETWORK LAYER	- USER DEFINED MESSAGE BUFFERING
LOAD LAYER	- USER DEFINED MESSAGE DESCRIPTORS

NETWORK STATION
DATA TRANSMISSION, RECEPTION, AND STORAGE



LANES

USER INTERFACE

THE USER INTERFACE ALLOWS THE EXPERIMENTER TO:

- 0 CONSTRUCT ALTERNATIVE NETWORKCONFIGURATIONS
- 0 SELECTIVELY COLLECT AND ANALYSE DATA
- 0 CONSTRUCT AND RUN MULTIPLE SEQUENTIAL EXPERIMENTS

THE USER INTERFACE PROVIDES:

- 0 USE OF "MENU" SYSTEM TO MANIPULATE LANES PARAMETERS
- 0 AN ON-LINE "HELP" UTILITY
- 0 A HARDCOPY USER'S GUIDE

LANES
DATA COLLECTION AND ANALYSIS SERVICE

COLLECTION SERVICES: STATION LEVEL

- 0 NUMBER OF OCCURRANCES OF ELEVEN PARAMETERS
- 0 MAXIMUM, MINIMUM, AND MEAN VALUE OF ELEVEN PARAMETERS
- 0 INTERVAL BASED COLLECTION OF TWENTY-ONE PARAMETERS
- 0 EVENT TIME TRACES OF ALL STATION ACTIVITY

COLLECTION SERVICES: NETWORK LEVEL

- 0 NUMBER OF OCCURRANCES OF ELEVEN PARAMETERS
- 0 MINIMUM, MAXIMUM AND MEAN VALUES OF TEN PARAMETERS
- 0 INTERVAL BASED COLLECTION OF TWENTY-ONE PARAMETERS

ANALYSIS SERVICES:

- 0 NETWORK THROUGHPUT EFFICIENCY
- 0 TOTAL BUS UTILIZATION

Topological Design of Fiber Optics Local Area Networks With Application to Expressnet*

by

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Computer Systems Laboratory

Department of Electrical Engineering

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Abstract

The use of fiber optics technology as a transmission medium in Local Area Networks (LAN's) brings about primarily three benefits: high bandwidth, immunity to electromagnetic interference, and light weight. But in (multi-tapped) passive broadcast bus configurations, the characteristics of certain fiber optics components that are needed, (such as reciprocity and excess loss in optical taps,) place severe constraints which must be taken into account in the topological design of such networks. These constraints manifest themselves in the form of a limitation on the maximum number of stations that a particular network configuration can support, given the components' characteristics and special requirements introduced by the access scheme. In this paper we provide a general and unified approach to the power budget analysis and optimization problem, and apply the technique to the study of a number of interesting high-performance LAN's, among others, Expressnet.

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*This work was supported by the National Aeronautics and Space Administration under Contracts NASA-NAG-2-292 and NASA-NAGW-419. M. Mehdi Nassehi is on an IBM Graduate Fellowship.

†On leave from Northwestern University, Dept. of Electrical Engineering and Computer Science, Evanston, IL, 60201.

VI. Conclusion

A number of configurations for fiber-optics implementation of Expressnet, and other related networks, were presented. Based on a unified approach, the maximum number of stations N_{max} that each of these configurations can support was computed.

For local area networks such as Expressnet, it proved useful to make a distinction between the *connectivity* requirement needed for broadcast communication and the *linear ordering* requirement needed for access control. Such a distinction allowed us to consider configurations consisting of two separate subnetworks: one called the *data subnetwork* satisfying the connectivity requirement, and the other called the *control subnetwork* satisfying the linear ordering requirement. The topology of the control subnetwork is inherently *linear*. When the topology of the data (collection) subnetwork is linear, then the latter automatically satisfies the linear ordering requirement and a separate control subnetwork becomes unnecessary.

The numerical results have shown that, with multimode fibers, high-cost components, and uniform optimization of couplers, all fiber-optics configurations implementing Expressnet can support more than 50 stations, with the exception of the all-linear configuration (i.e., linear collection and linear distribution) which can support 30 stations. For configurations in which the *data (collection) subnetworks* do not have a linear topology (i.e., tree, star, or compound), the number of stations that these data subnetworks can support (discarding the control subnetwork) far exceed 50, reaching several hundreds. The limitation of 50 to 70 stations, depending on the data rate (50 Mbps to 200 Mbps,) is then imposed by the linear control subnetwork. For components with mid-range parameters, only data subnetworks with the star topology and compound topologies (with large funneling width) can support large numbers (also in the hundreds). All others including the linear control subnetwork can hardly reach 10. Low cost components in all cases are totally inappropriate.

The numerical results have also shown that individual optimization substantially improves the number of stations, doubling it in many cases (obviously, with the exception of the star network where no 2×2 coupler is used.) It was observed that the singlemode fiber technology does not outperform the multimode case, despite the lower excess-loss of couplers in the former. This is due to the fact that the amount of optical power that can be injected into a singlemode fiber is significantly smaller than what can be injected into a multimode fiber.

From these results, it is clear that there are configurations in which one can support a significant number of stations, and that the main limitation comes from the linear ordering requirement imposed by the scheme. This suggests that the use of repeaters on the (fiber-optics) linear control subnetwork may be necessary to increase the maximum number of stations. This also suggests that, if one uses a medium other than fiber-optics (such as twisted-pair and coaxial cable) to implement the control subnetwork, then one could support a much larger number of stations than indicated.

The numerical results obtained for the data subnetworks, (excluding the control subnetwork,) are useful as they pertain to networks based on demand assignment access schemes that do not have the linear ordering requirement. Examples are PODA [34] and HAM [35] both of which achieve a high utilization of bandwidth by employing a reservation technique. Unfortunately these schemes tend to be more complex than the Expressnet access algorithm, and thus more costly to implement.

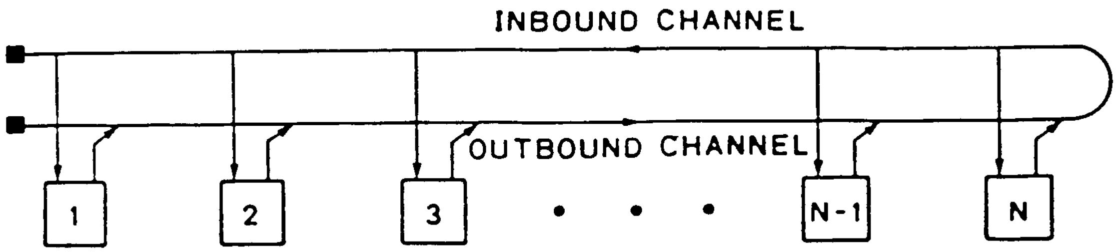

Fig. 2 The folded bus structure.

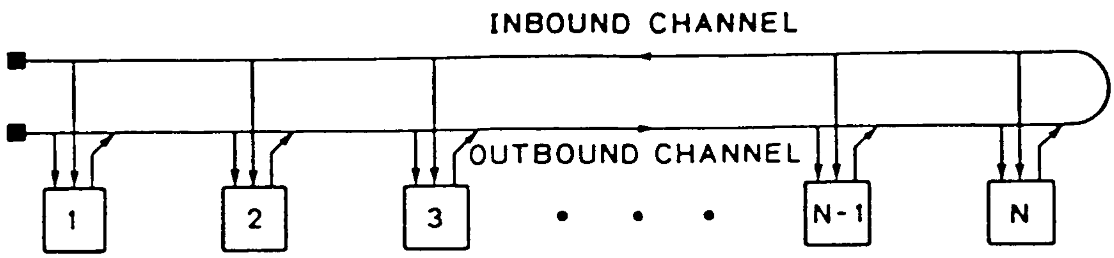

Fig. 3 The folded bus structure with sense taps on the outbound channel.

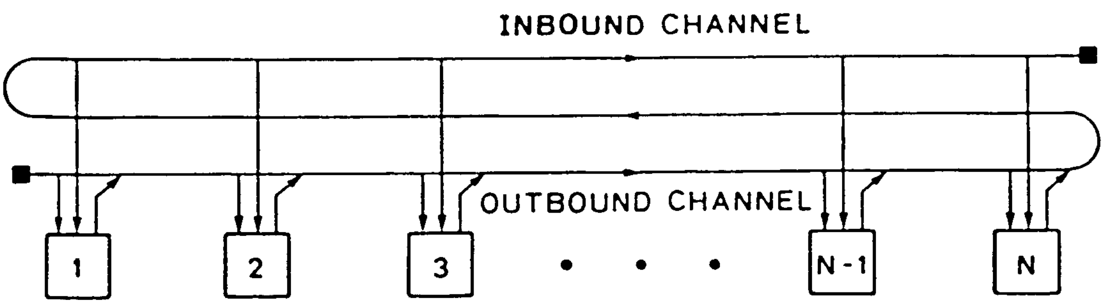

Fig. 4 UBS configuration used with Expressnet.

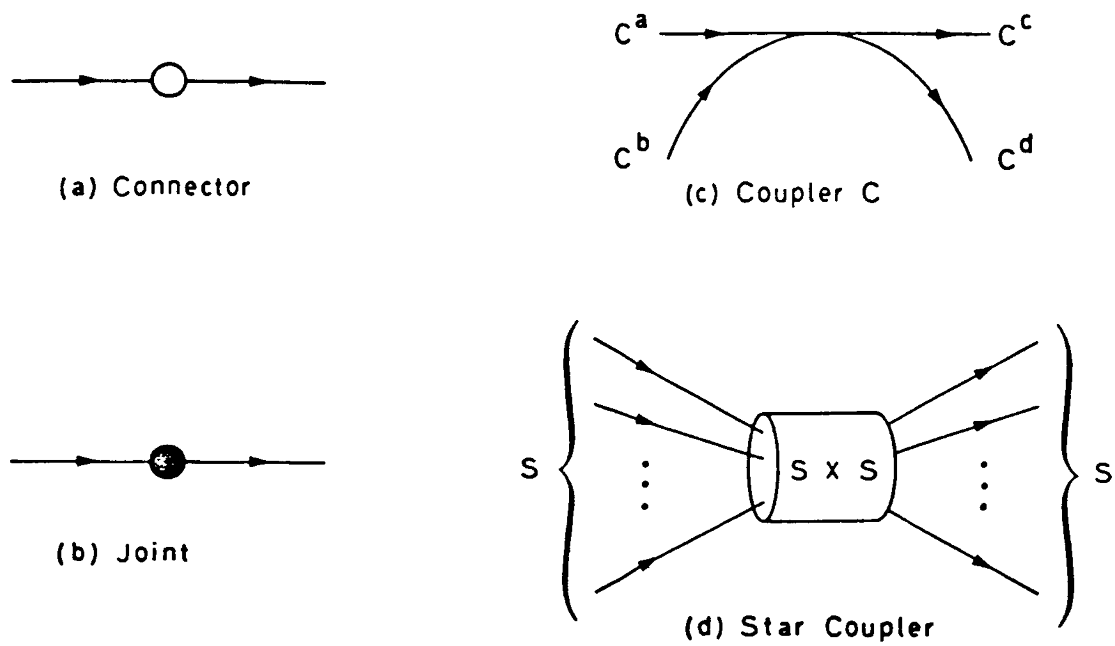

Fig. 5 Fiber-optics components: (a) a connector, (b) a joint, (c) a coupler, and (d) an $S \times S$ star coupler.

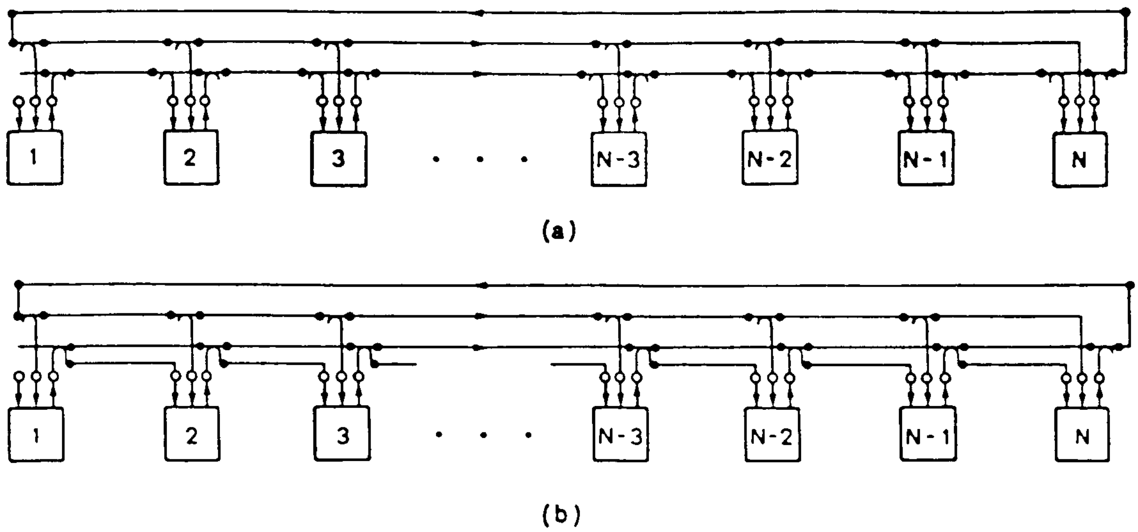

Fig. 6 Linear configuration (L).

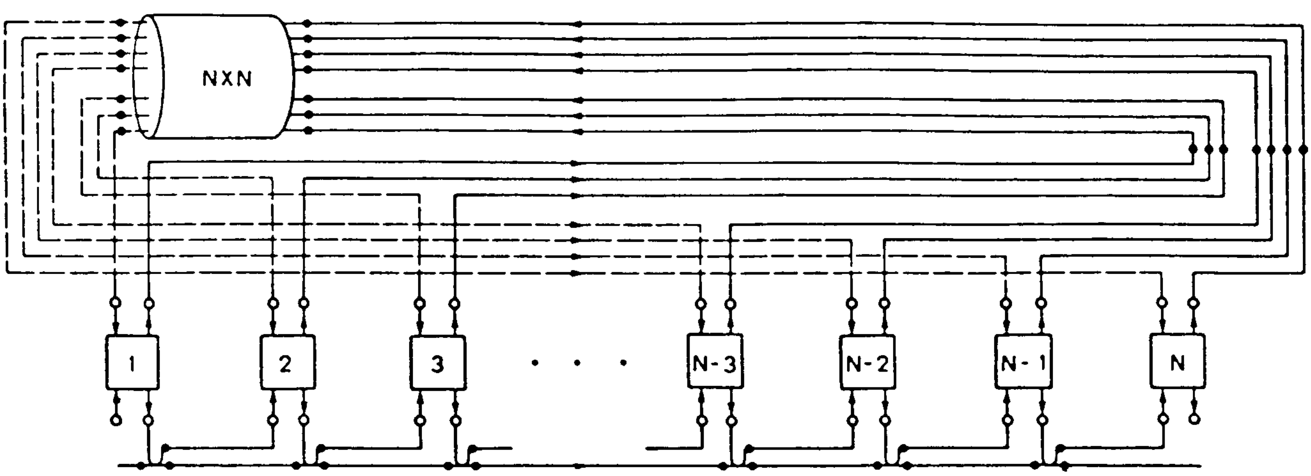

Fig. 7 Star configuration (S/C).

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IEEE TRANSACTIONS ON COMMUNICATIONS, VOL. COM-33, NO. 4, APRIL 1985

Coding and Decoding for Code Division Multiple User Communication Systems

TIMOTHY J. HEALY, SENIOR MEMBER, IEEE

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Abstract—**A new algorithm is introduced which decodes code division multiple user communication signals. The algorithm makes use of the distinctive form or pattern of each signal to separate it from the composite signal created by the multiple users. Although the algorithm is presented in terms of frequency-hopped signals, the actual transmitter modulator can use any of the existing digital modulation techniques. The algorithm is applicable to error-free codes or to codes where controlled interference is permitted. It can be used when block synchronization is assumed, and in some cases when it is not. The paper also discusses briefly some of the codes which can be used in connection with the algorithm, and relates the algorithm to past studies which use other approaches to the same problem.**

I. Introduction

THE primary purpose of this paper is to introduce a new algorithm for decoding signals in a code division multiple user communication system. We also discuss some concepts relating to coding for such systems, review some past work in coding and decoding, and show the relation of this work to the new algorithm introduced here.

The coding and decoding discussed here are applicable to many forms of multiple user systems, including many-to-one systems, usually referred to as "multiple access" systems, one-to-many, usually called "broadcast" systems, and any combinations of these. Code division multiple user communications can be an attractive alternative to other multiple user systems employing division over time or frequency if the system has a large number of customers with low duty cycles, so that a relatively small fraction of the customers are active users at any one time. In such situations it may not be desirable to dedicate a time or frequency slot to each customer.

Quite a bit of work has been done in this field in the past five years. Although this work is usually done for multiple access environments, it is very often applicable to other multiple user configurations also. The basic scheme discussed here was apparently first proposed by Viterbi [14]. The idea was then extended by Goodman, Henry and Prabhu [5]. Some approaches to coding were discussed by Einarsson [3]. An improvement in the decoding algorithm was proposed by Timor [12]. In addition to the above applications-related studies, a number of information-theoretic studies relating to this field have also been carried out, including [1], [2], [4], [8], and [10].

The decoding in the application studies above is accomplished by an approach which we shall refer to here as "address decoding." This paper introduces an alternative decoding algorithm which we refer to as "composition decoding," for reasons which will be discussed shortly. This algorithm is more powerful than address decoding in the latter's original form, but is essentially equivalent to the extended algorithm of Timor [12].

The algorithm introduced here can be used with error-free codes or with codes where controlled interference is permitted. It can be applied in situations where block synchronization is required, or it can be used where block synchronization is not available.

We begin by introducing the assumed channel model in Section II. In Section III the signaling scheme is introduced, and a definition which is important to the description of the composition decoding algorithm is given. The algorithm is described in Section IV. The problem of generating codes is discussed in Section V, and the new algorithm is related to address decoding. Error correction approaches are raised in Section VI, and Section VII gives a number of possible applications of code division multiple user coding.

Paper approved by the Editor for Communication Theory of the IEEE Communications Society for publication after presentation at IEEE GLOBECOM, San Diego, CA, December 1983. Manuscript received October 24, 1983; revised August 1, 1984. This work was supported by the National Aeronautics and Space Administration under Grant NCC2-128.
The author is with the Department of Electrical Engineering and Computer Science, University of Santa Clara, Santa Clara, CA 95053.

II. The Multiple User Communication Channel

In this section we describe the multiple user channel configuration, and make a number of assumptions about the channel.

A. System Configuration

The general multiple user communication channel considered here is shown in Fig. 1.

In the multiple access configuration there is more than one source, but only one receiver. In the broadcast mode there is just one source, but more than one receiver. The codes described in this paper are applicable to any of these forms, or to any combination of them, where k and s either are fixed over the life of the system, or are dynamic.

B. Assumptions

The channel assumed here is a so-called "OR" channel, in which the channel output is a zero (or a "space") if all of the inputs are zero, that is, if none of the k users radiates a signal into the channel, and the channel output is a one (or a "mark") if *one or more* of the users radiates into the channel. In a logical sense this is equivalent to an "inclusive or" operation. The output is zero only if all inputs are zero. Otherwise it is a one.

Other channels might be considered for the coding scheme introduced here. For example, an "adder" channel tells the receiver *how many* users radiated into the channel. This information can be used to increase the overall rate at which data are transferred. Nonetheless, the OR channel was selected here because it is simple, and because it is robust in a noisy environment. The general coding and decoding technique could be extended to other channels if desired.

We also assume block synchronization at first, but this is relaxed later in the paper.

III. The Signaling Scheme

This section describes the signaling which is assumed here, and introduces a definition which is important to the discussion of the new algorithm in the section to follow.

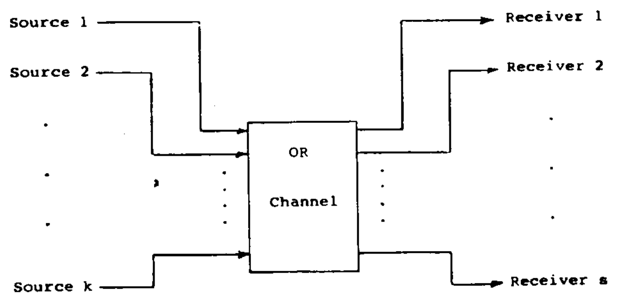

Fig. 1. Multiple user communication channel.

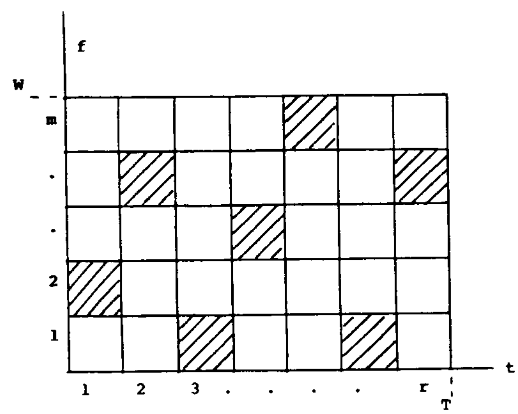

Fig. 2. General signaling scheme.

A. Signaling

The basic signaling technique considered in this paper is a frequency hopping scheme, shown in Fig. 2. During each of r time periods in a block of time of length T, a given user transmits exactly one signal burst of one frequency, indexed from 1 to m. Thus, each user creates a block of "on–off" or "mark–space" signals which represent the message to be sent. Each of the other users in the multiple access system simultaneously transmits some other block. The blocks which are transmitted are taken from a codebook which gives unique codewords or patterns to each user. The blocks are combined in the OR channel to form what we shall refer to here as a "composite signal." The task of the receiver is to deduce from the composite signal which blocks must have been sent by which users. It must do this without error, in the noise-free case, in spite of the fact that some users will, in general, radiate into the same cell in Fig. 2 at the same time, causing interference or a "hit." This paper shows how a decoding algorithm can accomplish this error-free decoding with reasonable efficiency. We refer to this as "composition decoding."

The signaling scheme has been described above as a frequency-hopping technique. However, it is important to understand that it is by no means essential that the final modulation stage in an actual transmitter be a frequency hopper. While it is convenient to describe the coding and decoding steps from the frequency-hopping viewpoint, the actual signal could be transmitted over the desired channel by any desired modulation scheme. For example, the m by r signal matrix could be transmitted as a binary sequence of length mr using binary phase shift keying by simply stringing out the binary elements of the matrix, one row at a time.

We assume first that the system has both block and bit synchronization. Block synchronization means that each of the users transmits in the same relative time frame. Everyone transmits the first frequency in its codeword at the same time, from the receiver's perspective, the second frequency next, etc. Bit synchronization means that there is no overlap of signal duration from one signaling time to the next. Thus, bits which are contiguous in time do not interfere.

We also assume that adjacent channel interference and intersymbol interference can be neglected. The result of the above assumptions is that the only interference effect considered here is simultaneous use of the same channel. We shall refer to this phenomenon as a "hit." This is a normal and expected phenomenon, the effects of which are eliminated by the decoding algorithm.

B. Interference-Free Codebooks

To illustrate the operation of the system, we give next a very basic example. We assume that there are just two users, called X and Y, which can send either of two messages, called A and B. The chosen code uses four frequency slots ($m = 4$) and two time slots ($r = 2$). Each of the users is assigned a codeword for each message. Each codeword has a certain number of terms or "elements" which are the frequencies transmitted in each of the time slots. A listing of the codewords assigned to the users is called a "codebook." The codebook for this example is given in Table I. For example, the element pair "1, 3" in the table means that user Y sends message A by transmitting frequency 1 in time slot 1 and frequency 3 in time slot 2. In Fig. 3 we show the composite signal matrices seen by the receiver for the four possible combinations of messages sent by the two users.

The expression $XA - YB$ means that user X sent message A and user Y sent message B.

At this point we introduce a definition which concerns codebooks, and which we will need later when we introduce the decoding algorithm.

Definition 1: A codebook is said to be "interference-free" if every codeword has at least one element which does not belong to any composite to which the codeword itself does not belong.

The codewords in Table I were carefully chosen so that the codebook would be interference-free.

(An alternate possible name for codes defined above as interference-free is "salient" codes, taken from the fact that each codeword has at least one salient or distinctive feature.)

If the codebook is changed to that shown in Table II, we no longer have an interference-free code. For example, codeword YA does not have an element which does not belong to the composite $XB - YB$. We say then that the codeword YA has been "masked" by the interference because the composite contains all of the elements of the codeword. We shall see later that it is impossible for the basic decoding algorithm to eliminate a codeword which has been masked, and hence, an error is made.

If we wish to add more users or messages to the system, that is, enlarge the codebook, the codebook becomes very complex.

In the initial description of the coding scheme and the decoding algorithm, the channel is assumed to be noise-free, so that the description can concentrate on the interference-rejection features of the system. Also, it is common to assume in many multiple user systems that the interference effects dominate noise. However, later it is shown that the algorithm can be modified to correct for random errors in a noisy environment.

IV. The Composition Decoding Algorithm

In this section we introduce an efficient algorithm to detect multiple user signals of the form assumed in this paper. We also briefly describe a variation of the algorithm which could be used for the ADDER channel.

TABLE I
CODEBOOK FOR TWO-USER SYSTEM

Message	User X	User Y
A	1,2	1,3
B	3,4	2,4

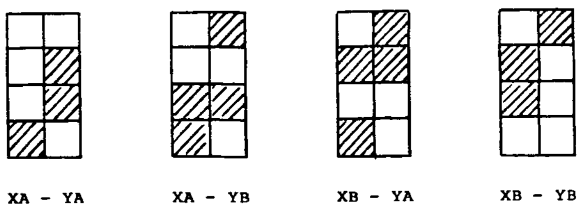

Fig. 3. Composite signal matrices seen by receiver.

TABLE II
A CODEBOOK WHICH IS NOT INTERFERENCE-FREE

Message	User X	User Y
A	1,3	2,4
B	2,3	1,4

A. The Decoding Task

It is possible to use brute force techniques to decode a composite signal, but the required systematic searches of all possible composites make the approach quite impractical.

Let us return to Fig. 2 to consider the dilemma faced by the receiver. Suppose that it finds that a particular square in the matrix is filled. It does not know how many users or which users radiated into that particular square. It is confused by the mutual interference phenomenon. The solution is suggested by an earlier theoretical study [8]. There it was shown that information is transferred to the receiver only if zero or one user radiates into a given square. The solution to the decoding problem is to concentrate not on the filled squares, but on the empty squares. Empty squares contain a great deal of information. They tell us that *the set of messages sent does not include any message with an element in that particular time and frequency square*. When we realize this, the decoding algorithm becomes quite simple.

B. The Composition Decoding Algorithm

We introduce the term "composition decoding algorithm" to identify the procedure described next. The receiver successively considers each time segment in the block (the columns in Fig. 2). To begin, it looks at the first column, noting which frequency squares are spaces. It then goes through the codebook and deletes every codeword which has an element corresponding to a space in the received composite signal, since these codewords could not have belonged to the set which made up the true composite signal. It then goes to the next time segment and repeats the process, deleting more codewords. After it has done this for all r time segments, there can be one and only one message left in each of the columns of the reduced codebook, and this message is that which the indicated user sent. The algorithm has successfully decoded the multiple access signal in spite of the mutual interference. We shall next prove that the algorithm cannot fail to correctly decode the composite signal if the code is interference-free.

C. The Decoding Algorithm Theorem

We assume the following situation. The active users each select one codeword and transmit it. The receiver sees a composite signal. For the particular received composite, the actual codewords which were sent by the users are called "proper codewords." This set will in general change every time block of length T as users select new messages to send. The codewords which did not make up a particular composite are called "improper codewords."

Theorem 1: For the algorithm to decode composite messages successfully, producing an error-free message set, it is a necessary and sufficient condition that the codebook be interference-free.

Sufficiency Proof: The algorithm removes only those codewords which have elements which are spaces in the composite signal. But proper codewords create marks where their elements appear. Hence, the algorithm cannot remove any proper codewords. Furthermore, every improper codeword must, by the definition of an interference-free codebook, have at least one element where the composite has a space. The algorithm will remove all of these improper codewords. Thus, an interference-free codebook is sufficient for yielding an error-free message set.

Necessity Proof: If the codebook is not interference-free, the algorithm will still leave all of the proper codewords in the reduced codebook. However, it will also leave all of those improper codewords which do not have at least one element which does not belong to the composite in question. Hence, a unique and unambiguous message set is not obtained, and the condition is seen to be necessary.

D. The Decoding Algorithm for an ADDER *Channel*

In an ADDER channel it is assumed that the receiver knows how many users radiate into a given signal element. For this channel the decoding algorithm is exactly the same as above. If the code is interference-free and there is no noise, there can be no errors. The advantage of the ADDER channel is in its enhanced ability to correct errors due to interference and noise.

V. THE GENERATION OF INTERFERENCE-FREE CODES

If the decoding algorithm is to decode composite signals successfully, it is necessary that interference-free codes be obtained. In this section we briefly introduce some codes which we claim to be interference-free. Because the primary focus of this paper is the decoding algorithm, we will not prove here that the codes are interference-free. This proof will be given in a subsequent paper which will focus on the generation of codes. We also consider the relation of these codes to other codes which have been reported in the literature.

A. Prime Number Codes

Tables III and IV give examples of two simple interference-free codes. The reader may wish to verify that these codebooks satisfy the definition of interference-free codes. For reasons which will be discussed shortly, we refer to these as "prime number codes" of order r, where in these examples r is 2 and 3, respectively.

A prime number code is defined here as a code which provides r codewords, each of which has r elements, to each of r users, where the jth codeword of the nth user is the vector

$$\overline{c_{jn}} = [j, j+n, j+2n, \cdots, j+(r-1)n]$$
$$j, n = 0, 1, 2, \cdots, r-1 \qquad (5\text{-}1)$$

where r is prime, and where the algebraic operations in (5-1) are modulo r.

We give one additional example of a prime number code, in Table V, which is intended to help explain the discussion which follows.

TABLE III
PRIME NUMBER CODEBOOK ($r = 2$)

Message	User 0	User 1
A	0 0	0 1
B	1 1	1 0

TABLE IV
PRIME NUMBER CODEBOOK ($r = 3$)

Message	User 0	User 1	User 2
A	0 0 0	0 1 2	0 2 1
B	1 1 1	1 2 0	1 0 2
C	2 2 2	2 0 1	2 1 0

TABLE V
PRIME NUMBER CODEBOOK ($r = 5$)

Message	User 0	User 1	User 2	User 3	User 4
0	00000	01234	02413	03142	04321
1	11111	12340	13024	14203	10432
2	22222	23401	24130	20314	21043
3	33333	34012	30241	31420	32104
4	44444	40123	41302	42031	43210

We consider now the general case where r is any prime number. The column of vector codewords produce for user 0 can be written as an r-term constant vector:

$$\overline{c_{j0}} = [j, j, j, \cdots, j] \tag{5-2}$$

where j is the index for the chosen codeword.

The row of vector codewords for the r users corresponding to message 0 can be written as

$$\overline{c_{0n}} = [0, n, 2n, \cdots, (r-1)n] \tag{5-3}$$

where n identifies the nth user. From (5-1)–(5-3) it is clear that the jth codeword of the nth user can be expressed as

$$\overline{c_{jn}} = \overline{c_{j0}} + \overline{c_{0n}}. \tag{5-4}$$

That is, any codeword is the modulo-r sum of the vector on the left end of the codeword's row and the vector on the top of the codeword's column. For example:

$$[30241] = [33333] + [02413]. \tag{5-5}$$

We shall return to an alternative way of viewing prime number codes, which arises from (5-4), shortly. First, we give, without proof in this paper, some properties of these codes.

1) All of the elements of any codeword are either identical (in the case of user 0), or all different.

2) Within any column (a given user), the elements of any codeword differ from those of any other codeword in all r places.

3) Any two codewords of different users differ in exactly $r - 1$ places.

4) Every composite has one and only one complete row.

5) Prime-number codes are interference-free.

While prime number codes yield codebooks of any desired size, for r prime, they have significant disadvantages. The primary problem is that these codes do not make efficient use of the spectrum. To formalize this point, we define spectral efficiency as the ratio of the rate at which the users as a whole transmit data, to the maximum rate at which an OR channel can be used to transmit data. The latter is simply the number of squares or elements in the signaling matrix, since each of these is worth one bit (it is either a mark or a space). Since there are r users with r different messages, the rate at which they send data is r times the logarithm to the base 2 of r. Hence, the efficiency is

$$e = (r \log_2 r)/r \times r = (\log_2 r)/r. \tag{5-6}$$

TABLE VI
EFFICIENCY OF PRIME NUMBER CODES

Number of users	Efficiency
3	0.528
5	0.474
9	0.352
13	0.285

The value of the efficiency for a number of values of n is given in Table VI.

The reason that these codes are rather inefficient is that they permit only one frequency use per time slot. This severely restricts the number of possible patterns which are permitted.

The efficiencies noted in Table VI are valid if all r users are active. If only a fraction of them are active, the efficiency must be multiplied by this fraction to get an even lower efficiency. The advantage of the above codes is that they do guarantee interference-free signaling. The disadvantage is that to obtain this guarantee we must separate messages in form, at a substantial cost in spectral space.

It is interesting to see what happens if we make the signal space available to only one user. Suppose that we keep the restriction that only one frequency is to be transmitted each time period, and that we have an r by r signaling matrix. The single user then sends one of r frequencies in the first time slot, one in the second, and so on. The number of distinct signals which the user can send is r raised to the r power. Hence, the signaling efficiency is

$$\begin{aligned} e &= (\log_2 r^r)/r \times r \\ &= (\log_2 r)/r \end{aligned} \tag{5-7}$$

which is exactly the same as that for the r user case. Note, however, that the power transmitted by this single user is only $1/r$ of that transmitted by all of the users together in the r user case.

D. Prime Number Codes as Address Codes

In this section we introduce another way to consider prime number codes, which is interesting for two reasons. First, it introduces an alternative to the composition decoding algorithm introduced in Section IV, with certain advantages and disadvantages. Second, this alternate approach is closely related to a number of recent studies. It is important to show how these studies relate to the present work. This issue is addressed in Section V-E.

Let us go back to (5-4), again using the codebook in Table V to illustrate a general point. We rewrite (5-4), identifying its components as message and address.

$$\overline{c_{jn}} = \underbrace{\overline{c_{j0}}}_{\text{message}} + \underbrace{\overline{c_{0n}}}_{\text{address}}. \tag{5-8}$$

We can think of the codebook as composed not of r^2 codewords, but rather of r codewords which are found, for example, for $r = 5$, in the left-hand column in Table V, and r addresses which are the sequences found in the top row, for example, in Table V. Each address is assigned to one of the r users. The jth codeword of the nth user is then formed by adding, modulo r, the desired user address to the desired message vector.

We shall refer here to codes which have the form of (5-8) as "address codes" to distinguish them from other codes described in this paper. One feature of address codes is that they suggest a rather simple decoding algorithm.

Address Decoding Algorithm: To determine the codeword sent by a specific user, subtract from the index of frequencies in a given column in the composite signal the value of the address of the desired user in the given frequency column. The desired message is given by the only full row of elements in the resulting matrix.

It is appropriate at this point to make some comments on the comparison between composition codes and address codes before turning to a discussion of previous work on address codes.

In a noise-free environment, the address decoding algorithm and the composition decoding algorithm are equally effective in decoding signals of *individual* users without error.

E. Previous Work in Address Codes

In this section we review some of the work which has appeared in the literature, principally in the past five years, in the area of coded frequency-hopped signals, and address codes in particular.

We begin by mentioning a recent paper by Chang and Wolf [1] which assume a general frequency-hopping scheme much like that considered here. Two types of channel are studied, one of which is without signal intensity information, and is equivalent to the OR channel assumed here. The other uses intensity information, that is, it assumes that the receiver can tell how many signals were radiated into a particular signal cell. Techniques are given for constructing codes which are uniquely decodable in a noise-free environment. Unfortunately, the resulting codes require that all users be active if the decoding is to be correct. We do not wish to make this restriction, and hence, these codes are not useful here.

The concept of address coding appears to have been introduced first in the literature by Viterbi [14], who applied it to a proposed low-rate mobile communication system. Goodman, Henry and Prabhu [5] proposed a multilevel frequency shift keying system using coding, which is closely related to some of the approaches discussed in this paper. Specifically, they use addressing to translate repetition code messages into frequency-hopped codewords such as those found in the prime number codes discussed above, and they use an address decoding algorithm to recover the signals. They obtain the probability of error for a given number of interfering users assuming that user addresses are chosen randomly. Sometimes the interference leads to a failure to decode, yielding an error, and sometimes it does not. Hence, these codes are not interference-free. But they do tend to provide for higher efficiency than interference-free codes, at the cost of nonzero error probability.

The problem of address codes was studied by Einarsson [3]. Using Einarsson's terminology, a codeword is given by the vector:

$$\overline{y_m} = \overline{a_m} + \overline{x_m} \cdot \overline{1} \tag{5-9}$$

where x_m, the address of the message to be transmitted, has the range $[0, 1, 2, \cdots, (Q-1)]$, and Q is the number of frequencies available in the frequency-hopping system. The vector 1 is a unit vector, consisting of L 1's, where L is the number of time slots in a block. Finally, a_m is an address vector generated by

$$a_m = (b_m, b_m C, b_m C^2, \cdots, b_m C^{L-1}) \tag{5-10}$$

where b_m, which is uniquely assigned to a particular user, is an element of the Galois field of order Q, GF(Q). (For a view of Galois fields, see [3] or [9].) It is necessary that C be a primitive element of GF(Q). The algebraic operations in (5-9) are modulo Q. The maximum number of codewords is Q, and the maximum value of L is $Q - 1$. It is shown by Einarsson that the codewords generated by the above equation can have no more than one element in common. As with the prime number codewords, there are no common elements for a given user's codewords. Unlike prime number codes, however, the Einarsson codes have some codeword pairs from different users that have no common elements.

Einarsson obtained a bound for the error probability for the above code.

$$P_w \leqslant (Q-1)(M-1)(M-2)\cdots(M-L)/Q^L \tag{5-11}$$

where M is the number of active users.

F. Random Codes

The codes we have discussed so far have been deterministic. The prime number codes are interference-free, and so are the Einarsson codes as long as the number of users does not exceed the number of time slots. These codes have the advantage that they are guaranteed to be interference-free. However, this guarantee has a price. These codes are inherently inefficient, as we have seen, particularly if users have low duty cycles, which is precisely the situation in which one may want to use code division systems. In this section we discuss random codes which are more efficient in many applications, but are subject to interference.

Random codes can be created either by generating random addresses, and applying these as before, or by generating random codewords directly. In either event it is no longer possible to guarantee that the algorithms, either address or composition decoding, will successfully recover all of the user codewords. Depending on which codewords are arbitrarily chosen by the various users, it is possible that a given codeword may not have an element which does not belong to the received composite signal. We say then that this codeword has been "masked" by the composite. In that event, neither of the algorithms will be able to remove this codeword.

If the composition decoding algorithm does not have knowledge of the codewords of the other users, it cannot remove this form of interference. This is also true of the address decoding algorithm. However, if full knowledge of the entire codebook is available, the composition decoding algorithm can remove this interference with high probability. The required extension to the algorithm is explained in Section VI-B.

It was observed above that the basic address decoding algorithm can detect but not correct errors. Timor [12] suggested an augmented algorithm which makes use of the signals sent by other users to determine (*probably*) which of two or more signals indicated for a single user is correct. The augmented algorithm accomplishes essentially the same task as the variation in the composition decoding algorithm discussed earlier. Timor reported an improvement in the spectral efficiency of about 50–60 percent with the modified algorithm.

Subsequently, Timor [13] proposed an extension of the coding scheme in which more than one tone can be trans-

mitted at the same time by a given user. This gives flexibility to the system since the time slot length can be increased. It also yields an increase in the number of users for a given error probability.

It is important to note that if we use a random codebook and, hence, no longer require an interference-free system, we no longer need block synchronization between the various users. Of course, we also can no longer use knowledge of other user signals to help correct for errors. However, there are other approaches to error correction.

VI. Word Error Correction

As has been stated before, the primary purpose of this paper is to introduce a new decoding algorithm. Under certain circumstances this decoding is subject to error. In this section we very briefly sketch some approaches to correcting these errors. In a future paper we will discuss error correction techniques in detail.

A. Causes of Error

If the channel is noiseless and an interference-free code is used, no errors are made by the decoding. But if there is noise or if we use a random code or if both conditions hold, then errors may occur.

Errors due to noise appear in the form of a mark changed into a space, called a deletion, or a space changed into a mark, called an insertion. The former result in too many words being deleted from the codebook, and some users appear not to have transmitted. The latter result in too few words being deleted, and some users have more than one codeword candidate.

Errors due to interference in the case of random codes appear as masked codewords in addition to the proper codeword. The decoder is not able to tell which is the correct codeword. This is apparently the same situation as with insertions due to noise. However, it is sometimes desirable to use different error correction techniques.

B. Error Correction Techniques

The discussion so far has concerned signaling over a block of time length T, as shown in Fig. 2. It is possible to effect error correction within this block, or over a sequence of blocks. We begin with the former.

If insertions and deletions due to noise are anticipated, it is possible to extend the decoding algorithm. The first step is to require that the receiver make soft decisions, and store information about the level of confidence it has in its estimates (the distance the signal was from the threshold). If a codeword is found to be missing, the decoder inserts the most likely deletion, and retries the algorithm. This continues with other likely deletion candidates until a complete decoding is effected. This approach will probably correct the error, unless the deletion which is reinserted happens to lead to an apparently complete solution which is incorrect.

If more than one codeword is left in a user's column after decoding because of interference, the error can probably be corrected if the user has access to the codewords of the other users. The technique is simple. Suppose that a user has two candidate codewords. The decoder looks at each of the two separately, and at the decoded codewords of the other users. If all of the elements of either of the two candidate codewords belong to the composite made up of the other user codewords, then that candidate was masked, and must be the incorrect word. If both candidates were masked, the decoder cannot remove the ambiguity, and the error persists.

Another approach which can be used as an alternative or in addition to the above is a "parity" code scheme. In this approach each user uses every nth block to send not a codeword but a parity word corresponding to the modulo-m sum of the previous $n-1$ words, where m is the number of possible message codewords. If the decoder detects an error in the $n-1$ codewords, a single error is umambiguously detected since the decoder simply chooses that candidate which makes parity add up. If more than one error is made, the detector may be able to detect the error, and may not. A final approach might better be called "error avoidance." There are some situations in which a transmitting user may have knowledge of the other signals before it adds its own. It can then refuse to send a signal when it knows that one of its other words will be masked by the other users. One such case is for broadcast signals, where all user signals intended for different receivers are known to the transmitter. A second case is a local area network in which a user is able to read the composite signal on the line before deciding whether to add a new contribution.

VII. Applications and Conclusions

This paper has introduced a new algorithm for decoding signals in a code division multiple user communication system.

The general approach and, hence, the new algorithm have a wide range of applications. Such a system could, of course, be used in a radio multiple access application, or in a broadcast application where different signals are to be sent to different users. It can also be used by a single user, who can select codewords from a number of columns and send a composite representing a number of messages at one time. It may have cryptographic applications, because the interference will look much like noise to any eavesdropper who does not have a codebook or the address set. The approach can serve as the basic signaling protocol for a local area network, as a substitute, perhaps for contention schemes such as Ethernet. The advantage of this approach is that contention is not a problem. Users may "speak" simultaneously and the decoding will do the job of separating the simultaneous messages.

Many issues are still under study. One of these is an evaluation of the relative complexity of implementing this algorithm, compared to implementation costs for other approaches. A second question is that of the best codes for particular applications. Still another is the problem of the best error correction scheme. In general, the answer to each of these questions will depend very much on the particular application.

Acknowledgment

The author wishes to acknowledge the very helpful comments of Dr. D. Costello.

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N87-29154

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COMPUTER SCIENCE/DATA SYSTEMS TECHNICAL SYMPOSIUM

April 17, 1985

ADVANCED DIGITAL SAR PROCESSOR (ADSP)

JPL

Tom Bicknell

792-2523

JPL

ADSP

OBJECTIVES

- DEVELOP THE TECHNOLOGY REQUIRED TO MEET THE SAR PROCESSING NEEDS FOR MISSIONS IN THE LATE 1980's
- BUILD AND DEMONSTRATE A HIGH PERFORMANCE ENGINEERING MODEL FLEXIBLE ENOUGH TO BE EASILY ADAPTED TO A WIDE VARIETY OF SAR PROCESSING TASKS AND CAPABLE OF REAL-TIME OR NEAR REAL-TIME THROUGHPUT RATES

APPROACH

- IMPLEMENT SAR PROCESSING ALGORITHM ELEMENTS (FFT'S, MULTIPLIERS, MEMORY SYSTEMS, INTERPOLATORS, FUNCTION GENERATORS, ETC.) INTO A PROGRAMMABLE PIPELINE ARCHITECTURE
- USE ONLY COMMERCIALLY AVAILABLE INTEGRATED CIRCUITS TO MINIMIZE COST AND RISK
- OPTIMIZE ARCHITECTURE AND CIRCUIT DESIGN FOR THE BEST BALANCE OF TESTABILITY, FLEXIBILITY, AND EFFICIENCY

JPL

WHAT IS THE ADSP?

THE ADSP IS A VERY EFFICIENT DIGITAL SAR PROCESSOR IN TERMS OF PERFORMANCE PER UNIT DEVELOPMENT COST OR PER UNIT OPERATIONS COST

THE MOST COST EFFECTIVE SAR PROCESSING TECHNOLOGY CURRENTLY IN USE IS A MINI-COMPUTER WITH ARRAY PROCESSORS

COST ITEM		MINI-COMPUTER SYSTEM (WITH 4 AP)	ADSP
DEVELOPMENT/ACQUISITION COST ($K)		1000	5000
DEVELOPMENT COST ($K) PER MEGAFLOP		20	1
DATA PROCESSING OPERATIONS COST ($K) (PER 100 SECONDS OF DATA TAKEN)	SEASAT	8	0.2
	SIR-B	2	0.1
DATA PROCESSING COST ($K) FOR A 100 HR SIR MISSION:		7000	500

JPL

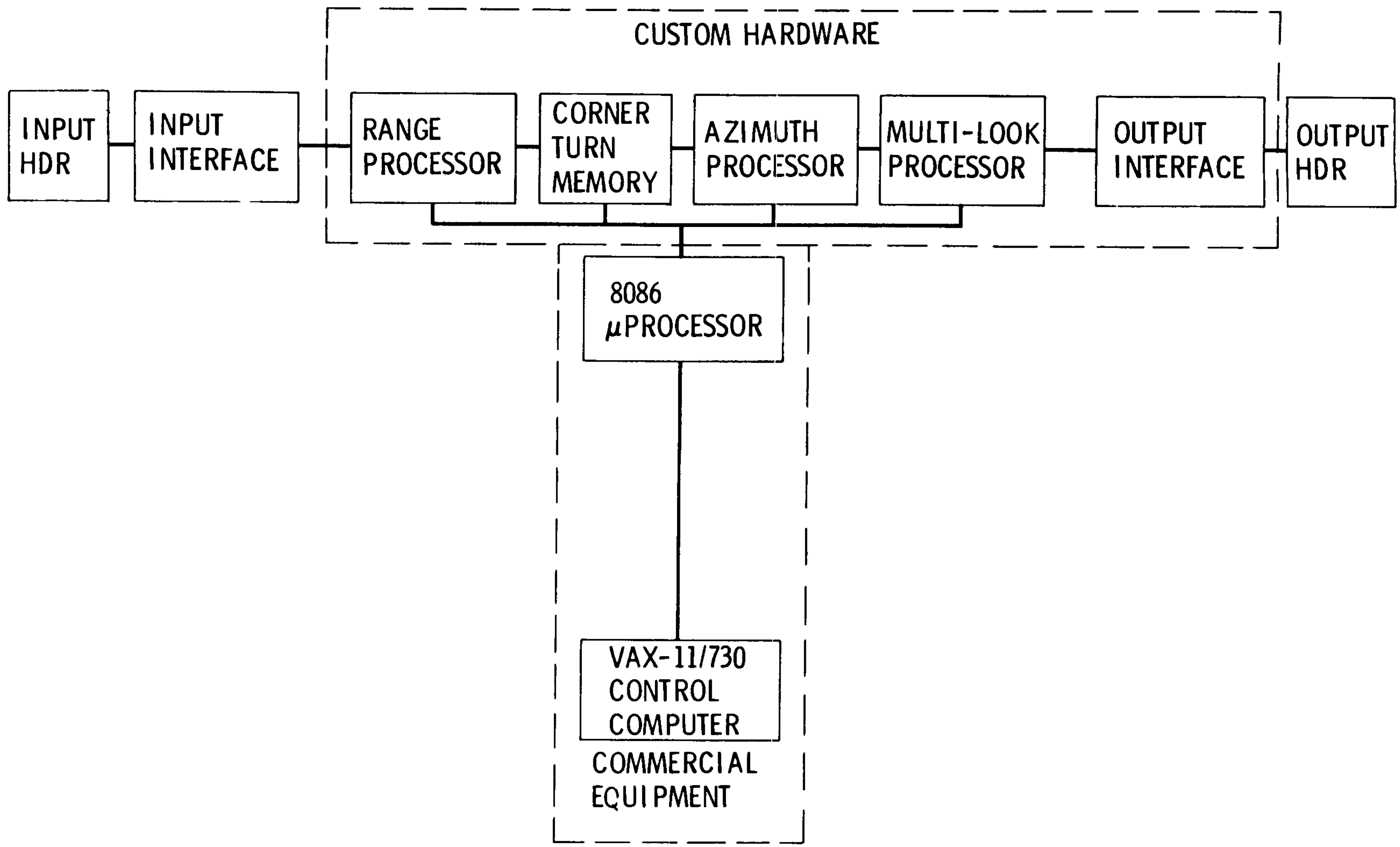
CURRENT AND FUTURE DATA PROCESSING TASKS

MISSION*	HOURS OF DATA TAKEN (EXPECTED)	MISSION PROCESSING COST $K	
		MINICOMPUTER-AP SYSTEM	ADSP
SEASAT (1978)	50	14,000	300
SIR-B OCT (84)	9	500	25
SIR-B' FEB '87	(50)	2,500	125
VRM 1988-89	(1200)	5,000	1,000
SIR-C 1989	(100)	10,000	400

*POTENTIAL SIR REFLIGHTS AND EXTENDED VRM MISSION NOT INCLUDED

JPL

ADSP ENGINEERING MODEL SYSTEM DIAGRAM



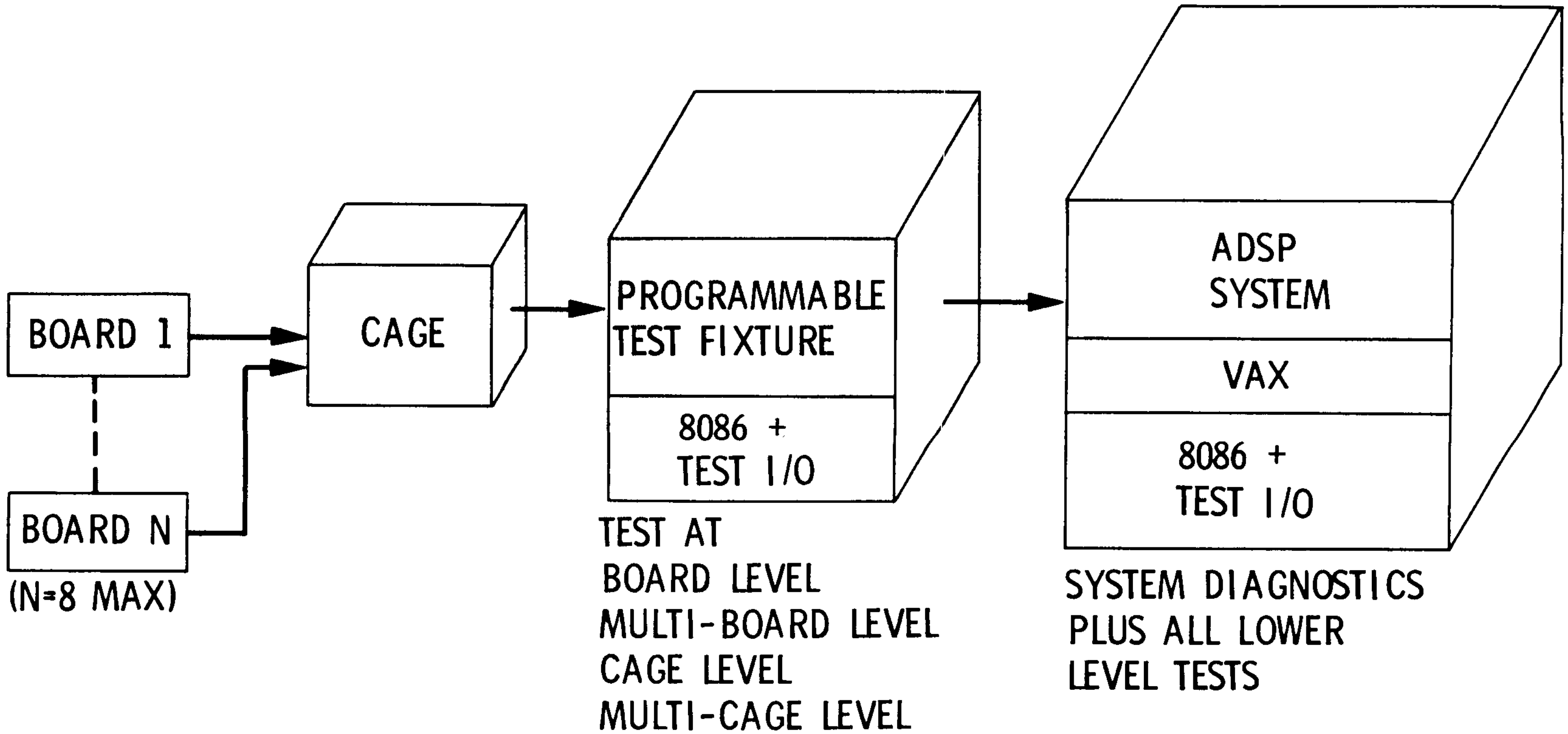
JPL

ADSP SYSTEM ATTRIBUTES

- 6 GIGAFLOP RATE AND 160 MEGABYTES OF MEMORY (~35,000 ICs)
- BUILT-IN DIAGNOSTICS
- PROVIDES FLEXIBLE SAR PROCESSING WITH VARIABLE: LOOKS, WEIGHTING FUNCTIONS, INTERPOLATION FUNCTIONS, AND PIXEL SPACINGS
- MULTI-LEVEL CONTROL CAPABILITY FROM AUTOMATED PRODUCTION DOWN TO MANUAL BIT MANIPULATION

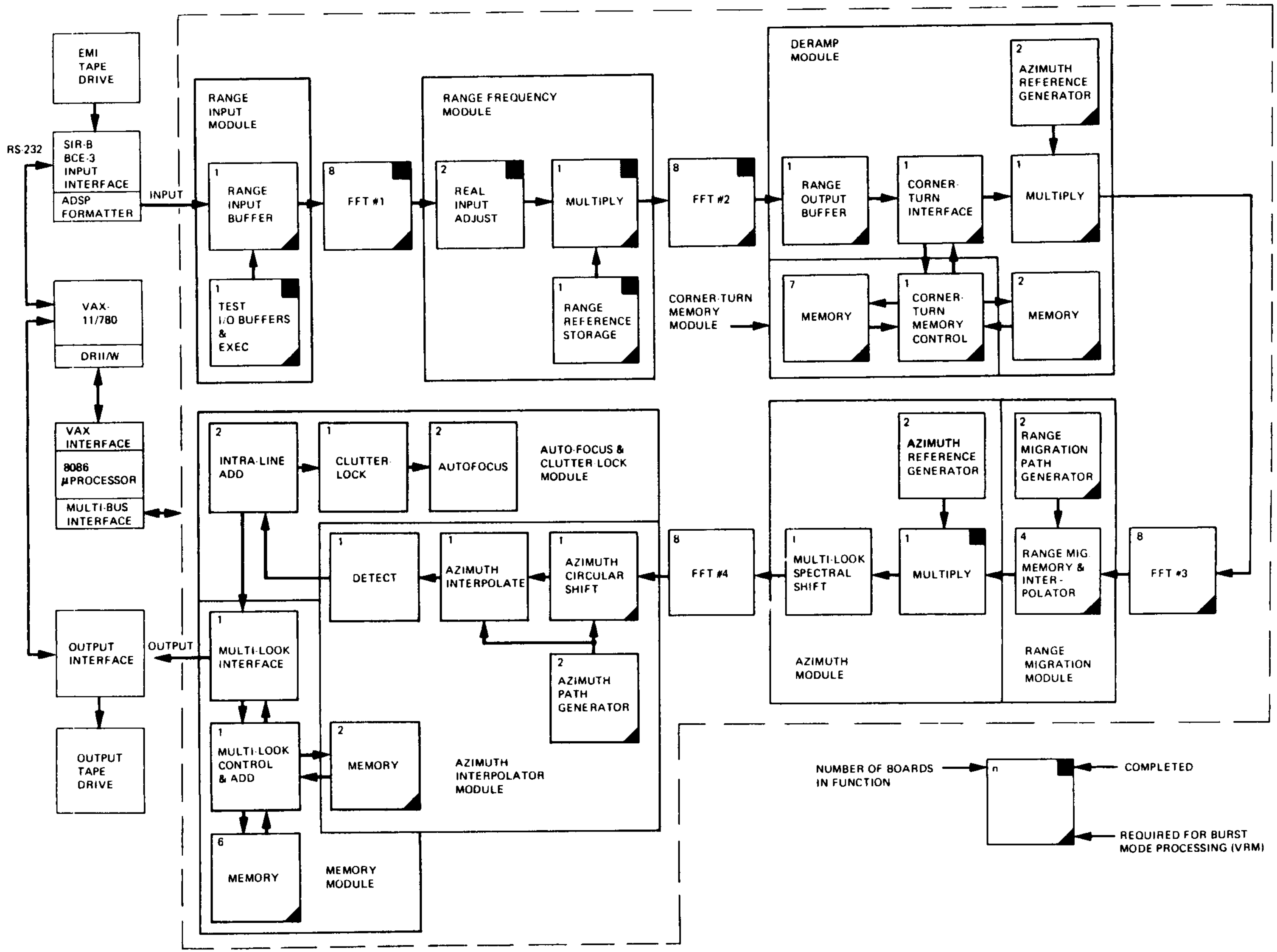
JPL

ADSP DEVELOPMENT TEST METHOD



JPL

ADSP HARDWARE BLOCK DIAGRAM



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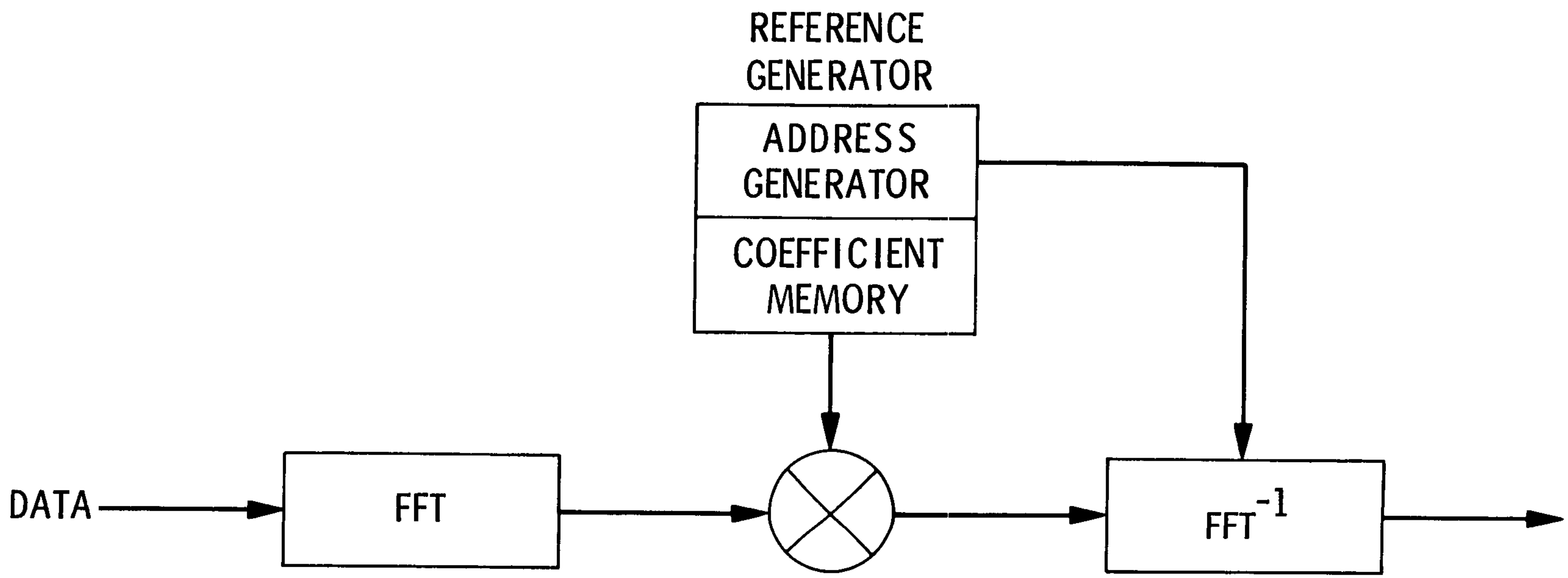
RANGE PROCESSOR



FFT MODULE

20 MHz PIPELINED FFT
PROGRAMMABLE UP TO 16K COMPLEX SAMPLES/LINE
22 BIT REAL, 22 BIT IMAGINARY (TRW FLOATING POINT)

REFERENCE GENERATOR

128K WORDS (12R, 12I)
LINEAR INTERPOLATE FUNCTION

JPL

OTHER USES OF ADSP

- SOME NON-SAR SIGNAL PROCESSING
- POWERFUL RESEARCH SAR PROCESSING
- TECHNOLOGY BASE FOR POTENTIAL ERS-1 PROCESSOR
- OPTIMIZED USE OF MATH AND MEMORY FUNCTIONS WILL AID GREATLY IN DESIGN OF FUTURE ON-BOARD SAR PROCESSORS

N87-29155

p.20

TESTING AND ANALYSIS OF DOD ADA LANGUAGE PRODUCTS FOR NASA

RTOP 506-58 AND 482-58

AN ACTIVITY IS DESCRIBED WHICH IS KEYED TO JSC'S ROLE AS AN ADA/APSE TEST SITE UNDER THE AUSPICES OF THE OAST AGREEMENT WITH DOD ESTABLISHING NASA/DOD COOPERATION IN THE STARS PROGRAM. I PROVIDED ELABORATION ON A CONTRACT WITH UH/CLC WHICH MINIMIZES USE OF LOCAL CONTRACTOR IR&D EFFORTS TO TEST AN EVALUATE ADA AND APSE FOR NASA. SPECIFIC OBJECTIVES AND CONCERNS RELATIVE TO POTENTIAL UTILIZATION OF ADA FOR SPACE STATION ARE DISCUSSED. FINALLY, DETAILED DISCUSSION IS PROVIDED IN REFERENCE TO STUDY TASKS SOON TO BE CONTRACTED OUT FOR DETAILED INVESTIGATION AND PROJECT RISK ASSESSMENT.

Johnson Space Center - Houston, Texas

TESTING AND ANALYSIS OF DOD ADA LANGUAGE PRODUCTS FOR NASA

RTOP #506-58

JOHNSON SPACE CENTER
AVIONICS SYSTEMS DIVISION
APRIL 1985

ENGINEERING DIRECTORATE — DESIGN•DEVELOPMENT•TEST	WHY IS NASA INVESTIGATING ADA	AVIONICS SYSTEMS DIVISION P. SOLLOCK — APRIL 1985

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0 SIZE AND COST OF SOFTWARE INCREASING SIGNIFICANTLY IN NASA SPACE FLIGHT SYSTEMS

0 NASA MUST REDUCE SOFTWARE DEVELOPMENT AND ESPECIALLY MAINTENANCE COSTS OF SOFTWARE OVER LONG LIFE-CYCLE PROJECTS

0 ADA IS STATE-OF-ART AND STANDARD DOD LANGUAGE DESIGNED FOR EMBEDDED COMPUTERS. (EMBEDDED COMPUTERS USED IN NASA SPACE FLIGHT SYSTEMS)

0 ADA WAS DESIGNED TO "REDUCE COSTS" IN DEVELOPMENT AND MAINTENANCE OF SOFTWARE FOR EMBEDDED COMPUTER APPLICATIONS :

- MANDATORY VALIDATION OF ADA COMPILERS PROVIDES :
  - REUSABLE SOFTWARE MODULES FROM ONE PROJECT TO ANOTHER EVEN IF DIFFERENT TARGET COMPUTERS ARE USED
  - PORTABLE SOFTWARE DEVELOPMENT/MAINTENANCE TOOLS (WRITTEN IN ADA)
- LANGUAGE FEATURES THAT REDUCE ERRORS :
  - HIGHLY STRUCTURED (MAKES BRANCHING HIGHLY VISIBLE AND MORE CONTROLLED)
  - READABLE (MORE DESCRIPTIVE KEY WORDS, STANDARD LANGUAGE, ETC.)
  - WELL-DOCUMENTED PROGRAMS (USER-DEFINED DATA TYPES, ALL DATA EXPLICITLY DEFINED, ETC.)
  - MORE ERROR CHECKING BY COMPILER BECAUSE PROGRAMMER MUST PROVIDE MORE EXPLICIT INFORMATION
- BUILT-IN AND AUTOMATED SOFTWARE CONFIGURATION CONTROL VIA HIGHLY INTEGRATED COMPILER, DATA BASE AND CONFIGURATION CONTROL TOOLS.

0 COSTS OF LANGUAGE DEVELOPMENT AND MAINTENANCE WILL BE SHARED BY DOD

PROJECT BACKGROUND

- O JSC RTOP APPROVED BY OAST IN JUNE 1983.

- O MEMO OF AGREEMENT SIGNED IN JUNE 1983 BETWEEN DOD AND OAST ESTABLISHING NASA/DOD COOPERATION IN DOD'S SOFTWARE TECHNOLOGY FOR ADAPTABLE, RELIABLE SYSTEMS (STARS) PROGRAM. JOINT JSC/UH-CL ADA/APSE TEST SITE AND EVALUATION PROJECT RECOGNIZED IN MEMO.

- O CONTRACT ESTABLISHED SEPTEMBER 1983 BETWEEN JSC AND UH-CL HIGH TECHNOLOGIES LAB TO :

  - PROVIDE GENERAL CONTRACTUAL BASIS FOR FUTURE SPECIFIC TASK AGREEMENTS WITH JSC IN SUPPORT OF RTOP.
  - PROVIDES SOURCE FOR ADA/APSE EXPERTISE AND CONSULTATION
  - ENABLES LOCAL-AREA CONTRACTORS TO COORDINATE THEIR IR&D EFFORTS THRU UH-CL IN SUPPORT OF JSC ADA PROJECT.

- O RESULT IS A JOINT JSC/FA&EA, UH-CL, AND LOCAL-AREA CONTRACTOR PROJECT TO TEST AND EVALUATE ADA AND APSE FOR NASA.

PROJECT OBJECTIVES

- O TEST AND EVALUATE ADA LANGUAGE AND TOOLS FOR THEIR APPLICABILITY FOR USE IN FUTURE NASA FLIGHT SYSTEMS.
  - -- TECHNOLOGY FOCUSED ON SPACE STATION
- O DEVELOP NASA STANDARDS AND POLICIES ON USE OF ADA.
- O DEVELOP PLANS AND GUIDELINES FOR TRANSITIONING FROM HAL/S TO ADA ON FUTURE NASA FLIGHT SYSTEMS.

MAJOR PROJECT TASKS	AVIONICS SYSTEMS DIVISION	
	P. SOLLOCK	APRIL 1985

1. INSTALLATION AND MAINTENANCE OF APSE'S
   - ESTABLISH JSC/DOD COORDINATION
   - INSTALL APSE'S ON APPROPRIATE JSC AND UH-CL COMPUTER SYSTEMS
   - GENERATE AND ESTABLISH APSE CONFIGURATION CONTROLS
2. ADA/APSE TESTING AND EVALUATION
   - PERFORM MATRIX ANALYSIS OF REQUIREMENTS VERSUS IMPLEMENTATION
   - INVESTIGATE APSE AND ADA TRANSPORTABILITY
   - EVALUATE PERFORMANCE AND CAPABILITIES OF ADA AND APSE BY BENCHMARK COMPARISONS WITH HAL/S AND ITS ENVIRONMENT.
3. DEVELOP PROTOTYPE SOFTWARE APPLICABLE TO NASA FLIGHT SYSTEMS
   - PROVIDE ADA TOOLS FOR USE BY LOCAL-AREA COMPANIES IN THEIR IR&D ADA PROJECTS RELATED TO JSC RTOP.
   - USE ADA AND APSE TO DEVELOP PROTOTYPE SOFTWARE FOR A DISTRIBUTED COMPUTER NETWORK IN THE SPACE STATION DATA MANAGEMENT SYSTEM TESTBED.
4. DEVELOP RECOMMENDATION REPORT ON SELECTION OF ADA FOR SPACE STATION FLIGHT SYSTEMS
   - IDENTIFY KEY PROBLEMS VIA MAJOR TASKS 2 AND 3.
   - PERFORM FOCUSED TECHNICAL STUDIES AND DEVELOP SOFTWARE PROTOTYPES FOR KEY PROBLEM AREAS
   - ASSESS RISK OF PROBLEM AREAS TO SPACE STATION PROJECT
   - DEVELOP ADA DECISION MATRIX
5. NASA STANDARDS AND TRANSITION
   - DEVELOP A NOMINAL SET OF STANDARDS AND POLICIES FOR USE OF ADA ON NASA PROJECTS
   - DEVELOP A PLAN FOR TRANSITIONING FROM THE HAL/S STANDARD TO ADA FOR AGENCY FLIGHT SOFTWARE PROJECTS

- 0 PROJECT MANAGER - JACK GARMAN (FD)
- 0 ASSISTANT PROJECT MANAGER - ED CHEVERS (EH)
- 0 PROJECT TECHNICAL MANAGERS - TERRY HUMPHREY (EH4)
  STEVE GORMAN (FD)
- 0 ADA/APSE CONSULTANT AND COORDINATOR OF PARTICIPATING LOCAL-AREA COMPANIES - DR. CHARLES MCKAY (UH-CL)
- 0 22 LOCAL-AREA COMPANIES DONATING IR&D RESOURCES: (ABOUT 70 HALF-TIME PERSONNEL)

BARRIOS TECHNOLOGY	LOCKHEED (LEMSCO)
BOEING AEROSPACE	MARTIN MARIETTA
CHARLES STARK DRAPER LABS	MCDONNELL DOUGLAS (MDTSCO)
COMPUTER SCIENCES CORP.	MITRE CORP.
DATA GENERAL	
FORD AEROSPACE	ROCKWELL INT'L
GRUMMAN DATA SYSTEMS	SINGER (LINK)
HARRIS CORP.	
HICKOK ELECTRICAL INSTRUMENTS	SOFTECH
IBM (FSD)	SPERRY UNIVAC
INTERMETRICS	TIMOTHY ALBERT AND ASSOC.
LITTON-MELLONICS	TRW

CONTINUING PROJECT ACTIVITIES

- MONTHLY JSC/UH-CL ADA STEERING GROUP MEETINGS WITH 22 PARTICIPATING COMPANIES.
  - STEER AND REVIEW STATUS OF PROJECT
  - REVIEW ADA TECHNOLOGY OBJECTIVES AND PLANS (ATOPs) WHICH DEFINE SUBTASKS TO BE PERFORMED BY PROJECT PARTICIPANTS.
- WEEKLY ADA/APSE TECHNICAL EXCHANGE MEETINGS BETWEEN UH-CL, JSC AND THE LOCAL PARTICIPATING COMPANIES.
- 64 ATOPs CURRENTLY DEFINED AND IN WORK BY 21 PARTICIPATING COMPANIES USING JSC AND UH-CL ADA SUPPORT TOOLS AND COMPUTERS.
- ADA/APSE TRAINING THRU UH-CL.

C-3

COMPLETED MILESTONES

DOD/NASA MEMO OF AGREEMENT ON STARS PROGRAM	JUNE 1983
JSC/UH-CL CONTRACT ESTABLISHED	SEPT 1983
JOINT JSC/UH-CL/LOCAL-AREA COMPANIES ADA STEERING GROUP ESTABLISHED	OCT 1983
COMMERCIAL NON-VALIDATED ADA SYSTEMS INSTALLED (TELESOFT, NYU-ADA/ED, INTEL 432)	JAN 1984
AIR FORCE/INTERMETRICS BOOTSTRAPPED ADA SYSTEM INSTALLED (NON-VALIDATED COMPILER)	FEB 1984
23 ATOPs SUBMITTED AND APPROVED	JUN 1984
ROLM / DATA GENERAL VALIDATED-ADA WORKSTATIONS LOANED TO JSC AND UH-CL	OCT 1984
ADA EVALUATION WHITE PAPERS COLLECTED FROM PROJECT PARTICIPANTS	NOV 1984
WHITE PAPERS CONSOLIDATED INTO LIST OF CURRENT PROBLEMS AND CONCERNS ABOUT ADA FOR SPACE STATION	DEC 1984
ARMY/SOFTECH VALIDATED-ADA SYSTEM (ALS) INSTALLED AT UH-CL, JSC, KSC, GSFC AND JPL	JAN/FEB 1985
64 ATOPs DEFINED AND IN-WORK BY 21 COMPANIES	FEB 1985
ATOP MINI-SYMPOSIUM AT JSC	FEB 1985
IDENTIFY KEY PROBLEMS WITH ADA/APSE FOR SPACE STATION PROJECT (INTERMETRICS AND JPL STUDIES)	FEB & APR 1985
COMPLETED BETA TESTING OF VAX ADA	MAR 1985

PROJECTED MILESTONES	AVIONICS SYSTEMS DIVISION	
	P. SOLLOCK	APRIL 1985

CONTRACTS AND ATOPS TO INVESTIGATE KEY ADA/APSE PROBLEMS AND ASSESS RISKS TO SPACE STATION PROJECT	APR 1985
DATA GENERAL/ROLM MV8000 ADE AND DEC VAX ADA PURCHASED AND INSTALLED AT JSC	JULY 1985
AIR FORCE/INTERMETRICS VALIDATED AIE INSTALLATION AT JSC AND UH-CL	SEPT 1985

NOTE! THE FOLLOWING MILESTONES ARE KEYED TO SPACE STATION PHASE B MILESTONES :

PROJECT REPORT AND RECOMMENDATION ON SELECTION OF ADA AS SPACE STATION LANGUAGE (PRIOR TO SSE RFP)	JAN 1986
SPACE STATION SOFTWARE SUPPORT ENVIRONMENT (SSE) REQUEST FOR PROPOSALS (RFP)	APR 1986
NASA ADA/APSE STANDARDS DEFINED (PRIOR TO SSE PDR)	NOV 1986
HAL/S TO ADA TRANSITION PLAN FOR SPACE STATION (PRIOR TO SSE PDR)	DEC 1986
SPACE STATION SDE PRELIMINARY DESIGN REVIEW (PDR)	JAN 1987

PROBLEMS/CONCERNS SUBMITTED THRU WHITE PAPERS PROVIDED BY PARTICIPATING CONTRACTORS (Nov. 1985)

CONSOLIDATED LIST GENERATED FROM WHITE PAPERS (Dec. 1985)

STUDY CONTRACTS BY INTERMETRICS AND JPL TO INDEPENDENTLY IDENTIFY KEY PROBLEMS FOR INVESTIGATION IN ORDER TO EVALUATE ADA FOR SPACE STATION (Feb. & Apr. 1985)

KEY PROBLEMS/CONCERNS IDENTIFIED AND TASKS SELECTED FROM CONSOLIDATED WHITE PAPER LIST AND INTERMETRICS/JPL STUDY REPORTS. FIVE STUDY CONTRACTS DEFINED TO INVESTIGATE THESE PROBLEMS AND TO ASSESS SEVERITY AND RISK TO SPACE STATION PROJECT IF ADA SELECTED.
(STUDY DURATION : May - Oct. 1985)

RECOMMENDATION REPORT ON SELECTION OF ADA FOR SPACE STATION TO BE GENERATED AND SUBMITTED (Jan. 1986)

ADA FOR SPACE STATION PROBLEMS AND CONCERNS	AVIONICS SYSTEMS DIVISION	
	P. E. SOLLOCK	APRIL 1985

(CONSOLIDATED LIST FROM WHITE PAPERS)

I. ADA LANGUAGE FEATURES AND CAPABILITIES (SUITABLE FOR IMPLEMENTING SPACE STATION REQUIREMENTS)

1 - FOR IMPLEMENTING REAL-TIME SOFTWARE FOR FAULT-TOLERANT,
1 DISTRIBUTED PROCESSING, AND HIGHLY RELIABLE SYSTEMS:
1 - COMPUTER AND NETWORK OPERATING SYSTEMS
1 (INTERRUPT HANDLING VIA ADA TASKING, ETC.)
1 - FAULT TOLERANT RECOVERY/RESTART SOFTWARE FOR MAN-RATED SYSTEMS
1 (EXCEPTION HANDLERS AND RECOVERY BLOCKS, ETC.)
1 - FLIGHT CONTROL SOFTWARE
1 (PRECISE CYCLIC PROCESSING SUPPORT, TASK ACTIVATION, SYNCHRONOUS
1 AND ASYNCHRONOUS TASK SCHEDULING, ETC.)
1 - COMMUNICATIONS AMONG ADA TASKS IN A DISTRIBUTED COMPUTER
1 (RENDEZVOUS CAPABILITIES AND EFFICIENCIES, ETC.)
2 - INTERFACING ADA WITH HAL/S AND OTHER LANGUAGES
3 - ADA LANGUAGE FEATURES WHICH HINDER TESTABILITY AND VERIFICATION OF
3 SOFTWARE FOR MAN-RATED SYSTEMS
3 (DYNAMIC MEMORY ALLOCATION, ETC.)

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II. ADA LANGUAGE STANDARDS

- DIFFERENCES IN OPERATION OF PROGRAMS GENERATED FROM THE SAME ADA SOURCE CODE BUT USING DIFFERENT VALIDATED ADA COMPILERS (DUE TO LACK OF COVERAGE IN ADA VALIDATION TEST SUITE AND LACK OF COVERAGE IN ADA LANGUAGE SPECIFICATION)
- IMPLEMENTED "OPTIONAL ADA FEATURES" NOT TESTED IN ADA VALIDATION TEST SUITE
- PERFORMANCE OF ADA TOOLS AND TARGET CODE NOT MEASURED BY ADA VALIDATION TEST SUITE

III. AVAILABILITY OF SUITABLE ADA TOOLS (TO SUPPORT TRAINING, PROOF-OF-DESIGN PROTOTYPING, AND DESIGN AND DEVELOPMENT SCHEDULES FOR SPACE STATION)

4 - TBD MINIMUM SET OF ADA TOOLS (MAPSE+) :
4 - VALIDATED COMPILER PLUS TBD OPTIONAL LANGUAGE FEATURES
4 - TOOLS FOR SPACE STATION TBD HOST COMPUTER/OPERATING SYSTEMS
4 - TOOLS/ENVIRONMENT COMPATIBLE WITH SPF HAL/S TOOLS/ENVIRONMENT
4 - MAPSE+ TOOLS SUPPORTING DISTRIBUTED HOST COMPUTER SYSTEMS
4 - TOOLS FOR SPACE STATION TBD TARGET COMPUTER/OPERATING SYSTEMS
4 - STATIC AND DYNAMIC ANALYSIS TOOLS FOR CONCURRENT TASKING
4 AND EXCEPTION HANDLING, ETC.
4 - SOURCE-LEVEL DEBUGGER FOR USER-INTERACTIVE DEBUGGING OF
4 CODE ON TARGET COMPUTER SYSTEMS.
4 - MAPSE+ TOOLS SUPPORTING DISTRIBUTED TARGET COMPUTER SYSTEMS TESTING.

(CONSOLIDATED LIST FROM WHITE PAPERS)

IV. LACK OF STONEMAN, CAIS, AND NASA STANDARDS TO SUPPORT :

- REUSABILITY/RETARGETABILITY OF ADA SOFTWARE FOR DIFFERENT TYPE TARGET COMPUTERS AND OPERATING SYSTEMS
  - NEED NASA PROGRAMMING STANDARDS FOR ADA
  - NEED INTERFACE STANDARDS BETWEEN TARGET CODE AND TARGET RUN-TIME SUPPORT SOFTWARE
- TRANSPORTABILITY AND INTEROPERABILITY OF MAPSES, APSES, OR PARTS THEREOF AMONG DIFFERENT TYPE HOST COMPUTERS AND OPERATING SYSTEMS.
- PORTABILITY OF PROGRAMMERS WITHOUT SIGNIFICANT RETRAINING AMONG DIFFERENT MAPSES/APSES (NO STANDARD USER INTERFACE)

V. AVAILABILITY OF TRAINED PERSONNEL (TO DESIGN AND DEVELOP SPACE STATION SOFTWARE USING ADA)

- TRAINED IN SOFTWARE ENGINEERING USING ADA
  - DESIGN PRINCIPLES APPLICABLE TO ADA
  - (SPACE STATION STANDARD?) ADA SOFTWARE DESIGN METHODOLOGY
- TRAINED IN ADA LANGUAGE
- TRAINED IN USE OF ADA (STANDARDIZED?) TOOLS FOR SPACE STATION
- SUFFICIENT NUMBERS AND TRAINING TO MEET SPACE STATION SCHEDULES

NOTE: "NUMBERS" IN LEFT MARGIN IDENTIFY "TASKS TO BE CONTRACTED OUT" FOR DETAILED INVESTIGATION AND PROJECT RISK ASSESSMENT.

(CONSOLIDATED LIST FROM WHITE PAPER)

4 - RUN-TIME SUPPORT LIBRARIES SUCH AS MATH FUNCTIONS, GRAPHICS, ETC.
4 - MATURITY OF ADA TOOLS
4 - IN CODE OPTIMIZATION
4 - SPEED AND SIZE OF PRODUCED TARGET CODE TO MEET REAL-TIME
4 TARGET COMPUTER REQUIREMENTS
4 - IN PROGRAMMER PRODUCTIVITY
4 - TBD MAPSE+ TOOLS SUPPORTING BOTH HOST AND
4 TARGET SYSTEMS.
4 - EXECUTION SPEED OF ADA TOOLS
4 (ESPECIALLY COMPILER AND LINKER/BINDER)
4 - DESCRIPTIVE AND SPECIFIC ERROR MESSAGES BY ALL TOOLS
4 - USER-FRIENDLY INTERFACE TO ALL TOOLS
4 - IN RELIABILITY
4 - OF ADA TOOLS AND LIBRARIES
4 - OF PRODUCED TARGET CODE AND RUN-TIME SUPPORT SOFTWARE

NOTE: "NUMBERS" IN LEFT MARGIN IDENTIFY "TASKS TO BE CONTRACTED OUT" FOR DETAILED INVESTIGATION AND PROJECT RISK ASSESSMENT.

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(CONSOLIDATED LIST FROM WHITE PAPERS)

VI. COSTS

(POSSIBLY PROHIBITIVE TO SPACE STATION PROJECT)

5 - COSTS OF ACQUIRING SUITABLE ADA TOOLS (SUPPORTING SPACE STATION
5 SCHEDULES) AND MAINTAINING TWO HOL SUPPORT SYSTEMS (HAL/S FOR SHUTTLE AND ADA
FOR SPACE STATION)

5 - COSTS OF REUSING AND MAINTAINING EXISTING HAL/S SOFTWARE IN ADA ENVIRONMENT
5 - RECODING FROM HAL/S TO ADA
5 - DEVELOPING, USE AND MAINTENANCE OF ADA TO HAL/S LANGUAGE INTERFACE STANDARD

5 - COSTS OF MAINTAINING SOFTWARE IF DUE TO ADA TARGET CODE PERFORMANCE
5 PROBLEMS, A SIGNIFICANT AMOUNT OF HAND-OPTIMIZATION IS REQUIRED IN
5 TIME-CRITICAL PARTS OF THE SOFTWARE.

- COSTS OF HIRING PERSONNEL WITH SUITABLE TRAINING IN ADA OR HIRING AND TRAINING SUCH PERSONNEL. (SEE "5. AVAILABILITY OF TRAINED PERSONNEL")

- COSTS OF MODIFYING REQUIRED NASA MANAGEMENT PROCEDURES AND DOCUMENTATION TO ACCOMMODATE ADA
  - NASA SOFTWARE ACQUISITION MANAGEMENT PLAN FOR ADA
  - NASA PROGRAMMING STANDARDS FOR ADA
  - OTHERS TBD

- COSTS TO NASA FOR MODIFICATION OF CONTRACTOR'S MANAGEMENT PROCEDURES AND DOCUMENTATION TO ACCOMMODATE ADA

NOTE: "NUMBERS" IN LEFT MARGIN IDENTIFY "TASKS TO BE CONTRACTED OUT" FOR DETAILED INVESTIGATION AND PROJECT RISK ASSESSMENT.

BENCHMARK SPEED COMPARISONS OF VALIDATED ADA SYSTEMS USING JSC DEVELOPED TEST PROGRAMS

	DEC VAX-ADA	DG/ROLM ADE	ARMY/SOFTECH ALS
COMPILE SPEED	1	3	17*
BINDER/LINKER SPEED	1	15	105*
EXECUTION SPEED	1	2	17*

"ADE" IS DATA GENERAL/ROLM ADA DEVELOPMENT ENVIRONMENT.
"ALS" IS ARMY/SOFTECH ADA LANGUAGE SYSTEM.
"*" DENOTES ONLY ABOUT 30% OF TESTS CASES COMPLETED ON ALS TO DATE.
27 TEST CASES RANGING IN SIZE FROM 44 TO 1189 LINES.
AVERAGE COMPILATION SPEED FOR VAX-ADA WAS 608 LINES/CPU MINUTE.
SPEED IS CPU TIME WITH SINGLE USER LOADING.
VAX 11/780 AND DG MV8000 COMPUTERS WERE USED AND ARE ASSUMED TO BE EQUIVALENT IN SPEED.

JSC ADA BENCHMARK TEST PROGRAMS

AVIONICS SYSTEMS DIVISION

P. SOLLOCK

APRIL 1985

NAME	# SOURCE LINES
SIMPLE IO TEST PROGRAM	44
FILE IO TEST PROGRAM	58
EXTENDED FILE IO TEST PROGRAM	203
FLOAT IO PACKAGE	428
FLOAT IO TEST PROGRAM	72
GENERIC FLOAT IO TEST PROGRAM	97
TERMINAL CONTROLLER PACKAGE	1261
TERMINAL CNTL TEST PROGRAM	266
STRING OPERATIONS PACKAGE	344
STRING TEST PROGRAM	98
MATRIX OPERATIONS PACKAGE	375
MATRIX TEST PROGRAM	208
TIMING FUNCTIONS PACKAGE	921
TIME FUNCTIONS TEST PROGRAM	125
DATASET BROWSE PROGRAM	493

NAME	# SOURCE LINES
DATASET RECORD SORT PROGRAM	261
DATASET RECORD SORT PROGRAM	261
MATH LIBRARY (SEQUENTIAL VERSION)	1189
SEQ MATH LIB TEST PROGRAM	364
SQRT ONLY TEST PROGRAM	282
EXP ONLY TEST PROGRAM	76
MATH LIBRARY (GENERIC VERSION)	1142
GENERIC MATH LIB TEST PROGRAM	360
DYNAMIC BUFFERING PACKAGE	186
DYNAMIC BUFFERING TEST PROGRAM	76
TASKING COMMUNICATION PACKAGE	302
TASK COMM TEST PROGRAM (COMMUNICATION)	117

REPRESNTATIVE ATOP'S	AVIONICS SYSTEMS DIVISION
	P. SOLLOCK — APRIL 1985

ATOP NUMBER	COMPANY	ATOP TITLE	ATOP STATUS
03-05-02	BOEING AEROSPACE	INVESTIGATE THE EFFECTS OF TRANSLATING AN EXISTING EXPERT SYSTEM/ ADA TRANSLATION SYSTEM TO THE ADA PROGRAMMING LANGUAGE	IN REVIEW
03-06-03	DRAPER LABS	ADA ARITHMETIC/ALGEBRARIC/ TRIGONOMETRIC RUN TIME LIBRARY	APPROVED
03-02-01	FORD AEROSPACE	ADVANCED MICROPROCESSOR NETWORK STUDY	APPROVED
02-03-01	IBM/FSD	ADA BETA TEST SUPPORT ACTIVITIES (ADA, HAL/S BENCHMARK PROGRAMS)	APPROVED
02-03-02	ROCKWELL, INT.	STUDY OF ADA IN CONCURRENT REAL-TIME PROCESSING	APPROVED

N87-29156

p. 22

AN OPTICAL DISK ARCHIVE FOR A DATA BASE MANAGEMENT SYSTEM

Computer Science/Data System
Technical Symposium

April 1985

Douglas T. Thomas
Marshall Space Flight Center

ABSTRACT

This presentation will provide an overview of a Data Base Management System (DBMS) that can catalog and archive data at rates up to 50M bits/sec. However, the detail emphasis will be on the laser optical disk system that is used for the archive.

All key components in the system (3 VAX 11/780s, a SEL 32/2750, a high speed communication interface, and the Optical Disk) are interfaced to a 100M bits/sec 16-port fiber optic bus to achieve the high data rates. The basic data unit is an autonomous data packet. Each packet contains a primary and secondary header and can be up to one million bits in length. The data packets are recorded on the optical disk at the same time the packet headers are being used by the relational data base management software ORACLE to create a directory independent of the packet recording process. The user then interfaces to the VAX that contains the directory for a quick-look scan or retrieval of the packet(s). The total system functions are distributed between the VAX computers and the SEL.

The optical disk unit records the data with an argon laser at 100 M bits/sec from its buffer, which is interfaced to the fiber optic bus. The same laser is used in the read cycle by reducing the laser power. The data is read from the disk at 100M bits/sec and placed in the unit's output buffer at 100 M bits/sec. The distribution rate from there to the user is controlled by the rate the user can accept the data.

EB663

AN OPTICAL DISK ARCHIVE FOR A DATA BASE MANAGEMENT SYSTEM

COMPUTER SCIENCE/DATA SYSTEMS
TECHNICAL SYMPOSIUM

DOUG THOMAS
MSFC

EB677

OBJECTIVE

DEVELOP AND DEMONSTRATE THE TECHNOLOGY REQUIRED TO ACCEPT DATA AT RATES UP TO 50M BITS/SECOND, GENERATE A DIRECTORY OF THE DATA, AND RECORD THE DATA IN A LARGE ONLINE ARCHIVE. THE DIRECTORY AND DATA COULD THEN BE ACCESSED IN NEAR REAL TIME THROUGH A DATA BASE MANAGEMENT SYSTEM.

EB678

PROBLEMS ADDRESSED

- HANDLING DATA AT HIGH RATES
- ARCHIVING LARGE VOLUMES OF DATA AT HIGH RATES
- REDUCING USER ACCESS TIME TO DATA AFTER IT HAS BEEN RECORDED ON GROUND.

EB679

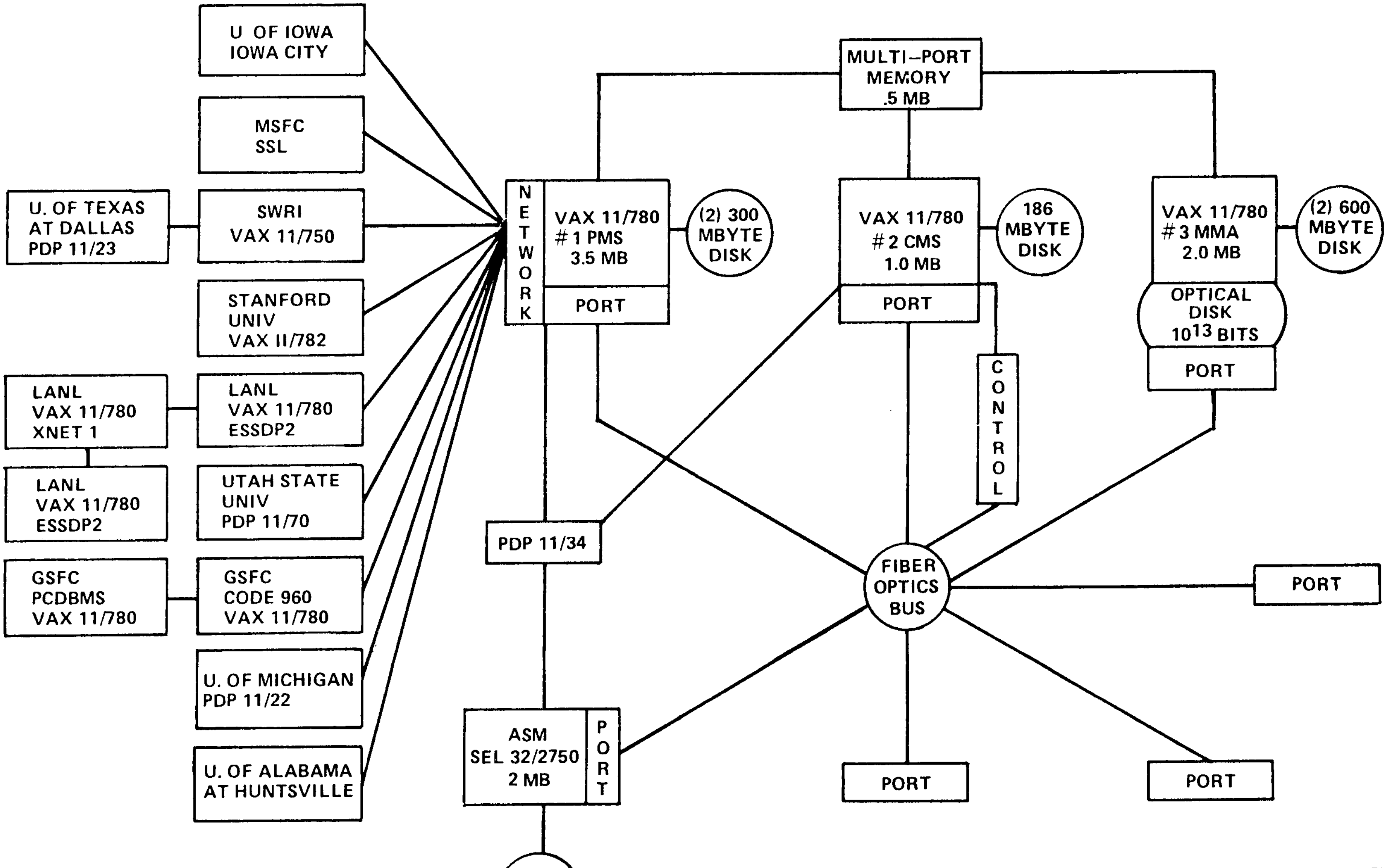
KEY SYSTEM ELEMENTS

- AUTONOMOUS DATA PACKET
  - MISSION AND SENSOR INDEPENDENT
- 16–PORT FIBER OPTIC DATA BUS
  - BY–PASS CONVENTIONAL COMPUTER I/O TO ACHIEVE HIGH DATA RATES
- OPTICAL DISK RECORDER
  - USE OF ARAGON LASER TO ACHIEVE HIGH DENSITY RECORDING AND AN AUTOMATED "JUKEBOX" TO PROVIDE A LARGE ONLINE ARCHIVE.

EB664

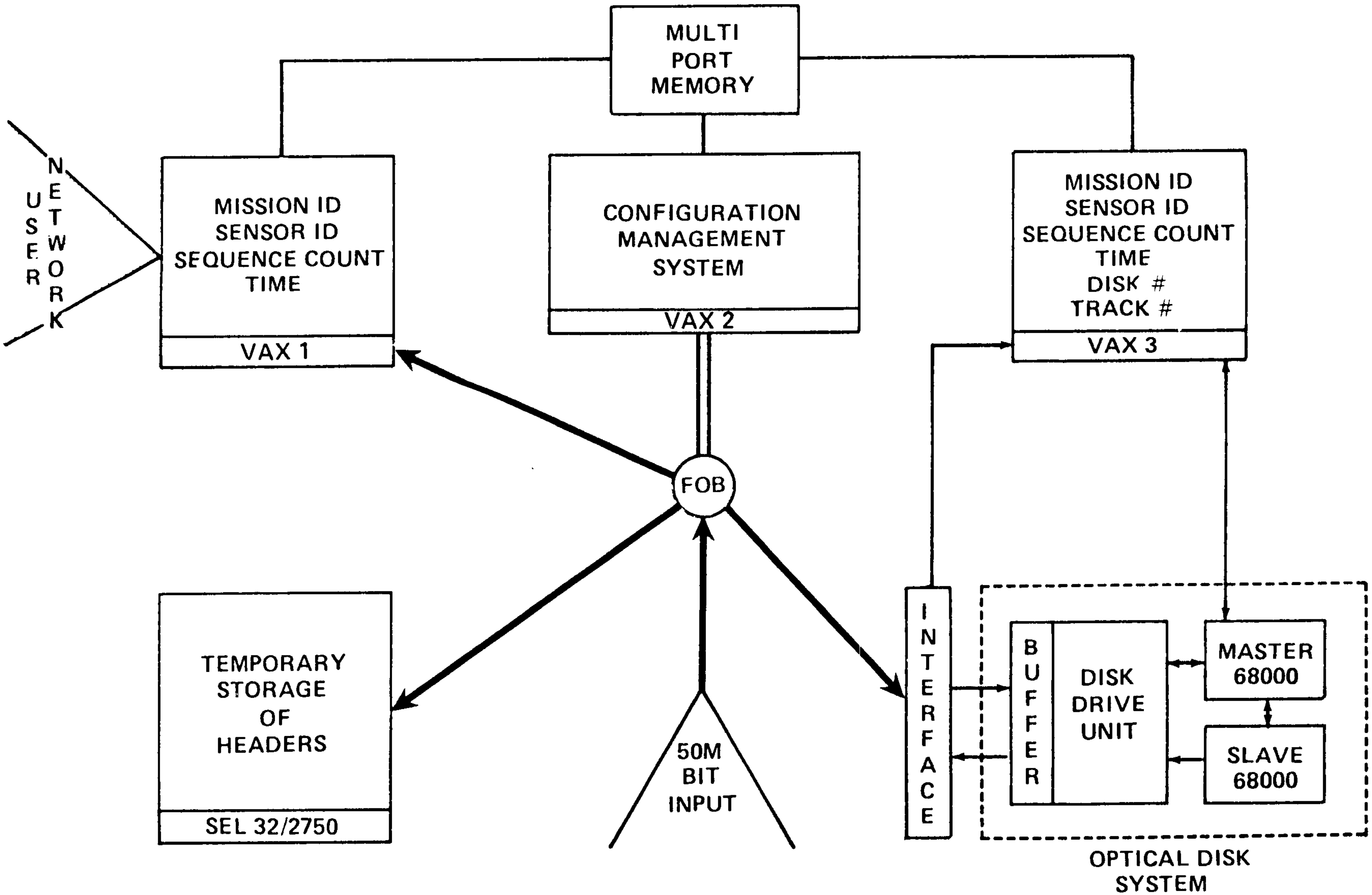
SPACE–PLASMA COMPUTER ANALYSIS NETWORK
(SCAN)

DATA BASE MANAGEMENT SYSTEM/MASS MEMORY ASSEMBLY
(DBMS/MMA)



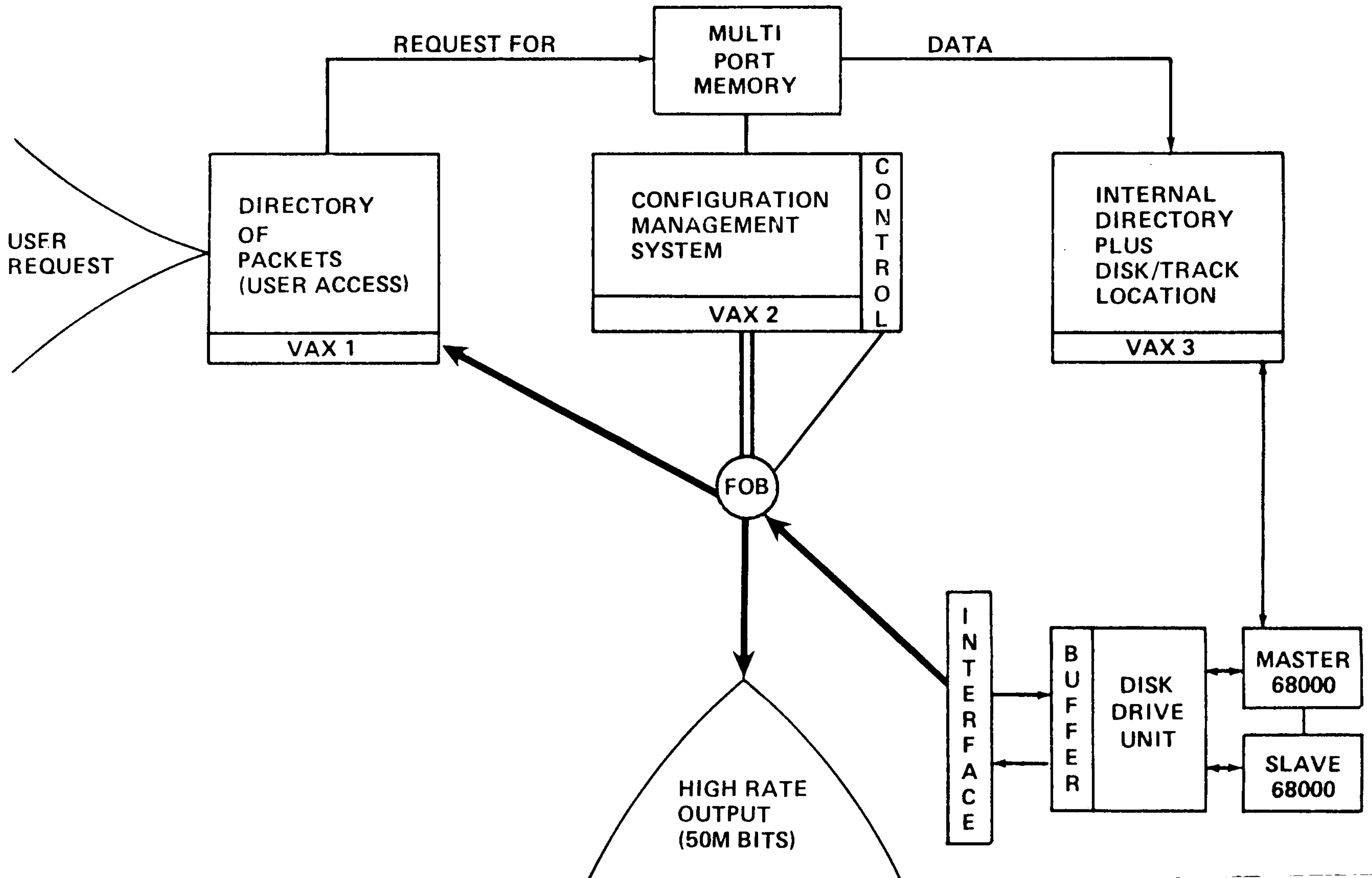
EB665

PRIMARY INPUT DATA FLOW



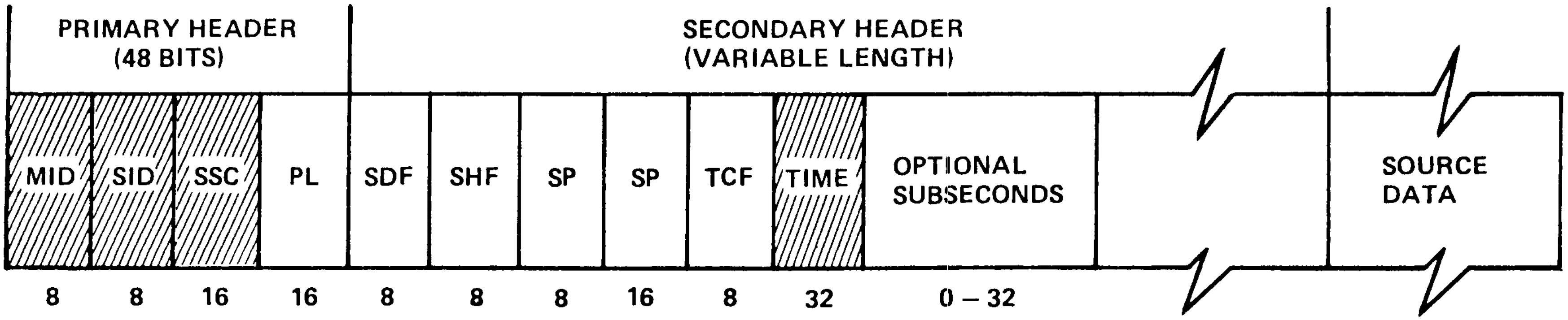
EB682

USER ACCESS TO DATA



EB666

DBMS PACKET FORMAT



MID — MISSION ID

SID — SOURCE ID

SSC — SOURCE SEQUENCE CONTROL
BITS 15 – 14: SEGMENT FLAGS
BITS 13 – 0: SOURCE SEQUENCE COUNT

PL — PACKET LENGTH (NUMBER OF 16 BIT WORDS IN THE PACKET – 1. THIS LENGTH DOES NOT INCLUDE THE PRIMARY HEADER)

SDF — SOURCE DATA FORMAT. THIS FIELD IS USED TO IDENTIFY THE INTERNAL FORMAT OF THE DATA WHICH IS CONTAINED IN THE SOURCE DATA FIELD OF THE PACKET.

SHF — SECONDARY HEADER FORMAT. THIS FIELD SPECIFIES BY WAY OF AN EXTERNAL LOOK–UP PROCEDURE THE FORMAT AND LENGTH OF THE SECONDARY HEADER.

SP — SPARE FIELD

TCF — TIME CODE FORMAT. BITS 0 – 3: TIME CODE ID
BITS 4 – 7: OFFSET VALUE

TIME – USER DEFINED TIME

//////// – PRIMARY SORT KEYS

OPTICAL DISK SYSTEM

EB673

OPTICAL DISK STATISTICS

	DESIGN GOALS	MEASURED DATA	UNITS
ON LINE CAPACITY	10^{13}	$.975 \times 10^{13}$	BITS
ACCESS TIME			
ANY DISK	6.0	6.8	SEC
LOADED DISK	0.5	0.66	SEC
DATA RATES	0–50	0–50	MBPS
BIT ERROR RATE	10^{-8}	10^{-8}	MICRONS
SPOT SIZE	.5	.5	MICRONS
SPOT SPACING	1.25	1.25	
DATA STRUCTURE	TRACK = REVOLUTION	TRACK = REVOLUTION	

- MASTER/SLAVE 68000 BASED CONTROLLER
- 14 INCH ALUMINUM DISK IN PROTECTIVE CARTRIDGE

EB667

SYSTEM UNITS

1. DISK DRIVE UNIT (DDU)

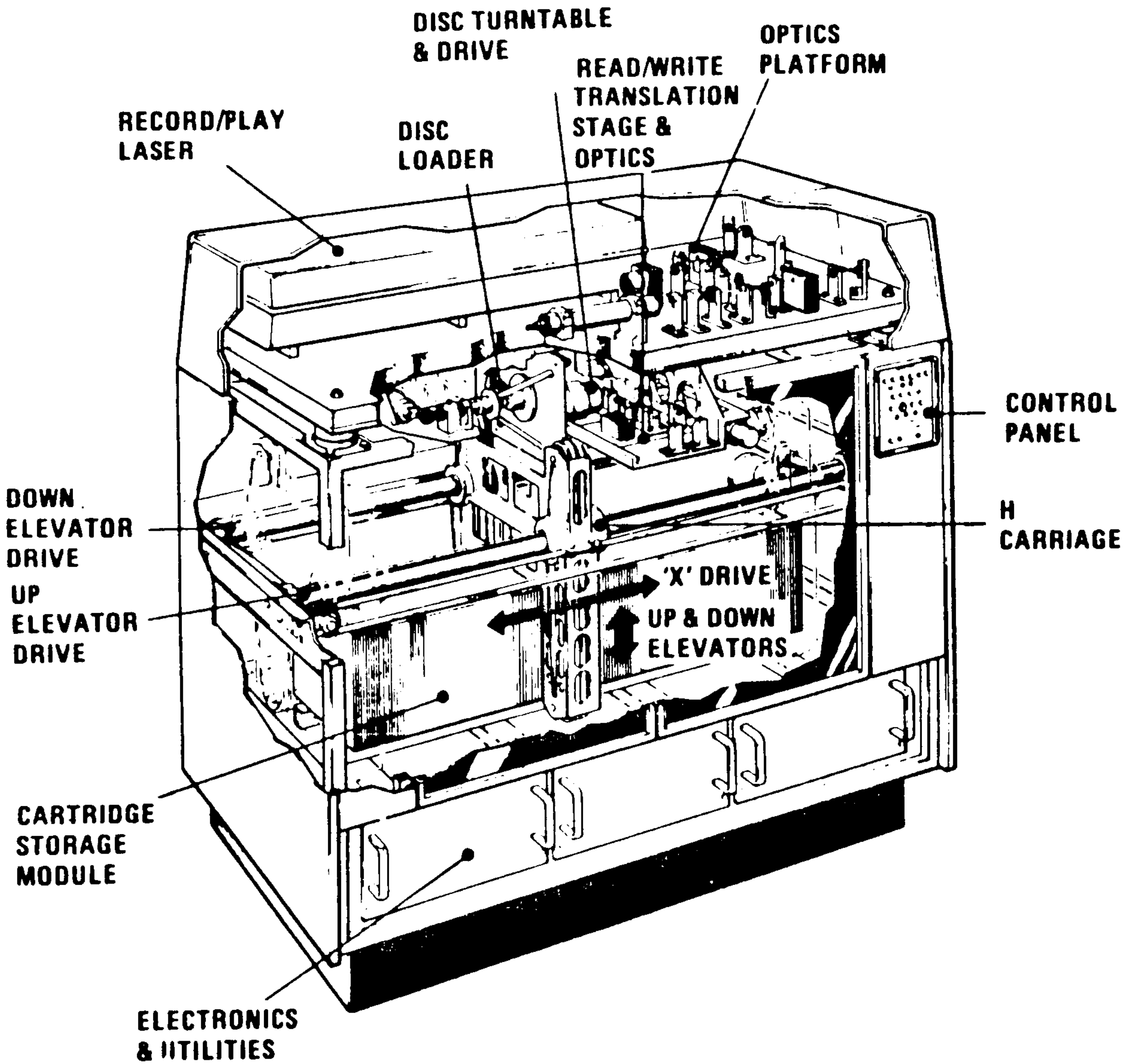
   - PERFORM ALL ELECTRO/OPTIC/MECHANICAL FUNCTION REQUIRED TO RETRIEVE DATA
   - WRITES TO AND READS FROM DISK
   - RETRIEVES AND STORES DISK IN JUKEBOX

2. HARDWARE/SOFTWARE CONTROLLER

   - INTERFACE TO HOST (VAX)
   - CONTROLS AND MONITORS ALL FUNCTIONS
     - TWO MOTOROLA 68000
   - DUAL INPUT BUFFERS – COMPENSATE FOR VARIABLE RATES

EB668

DISC DRIVE UNIT



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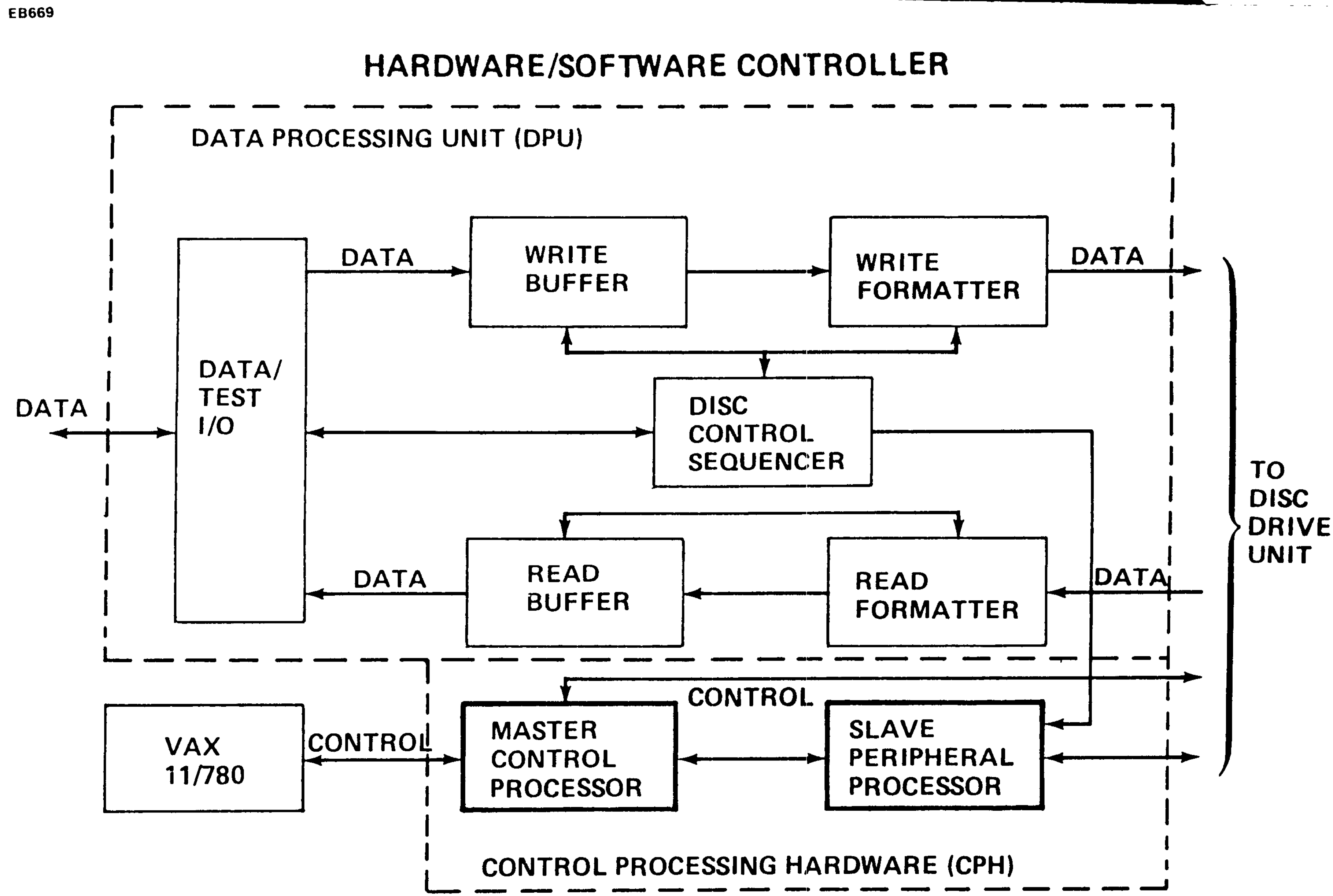
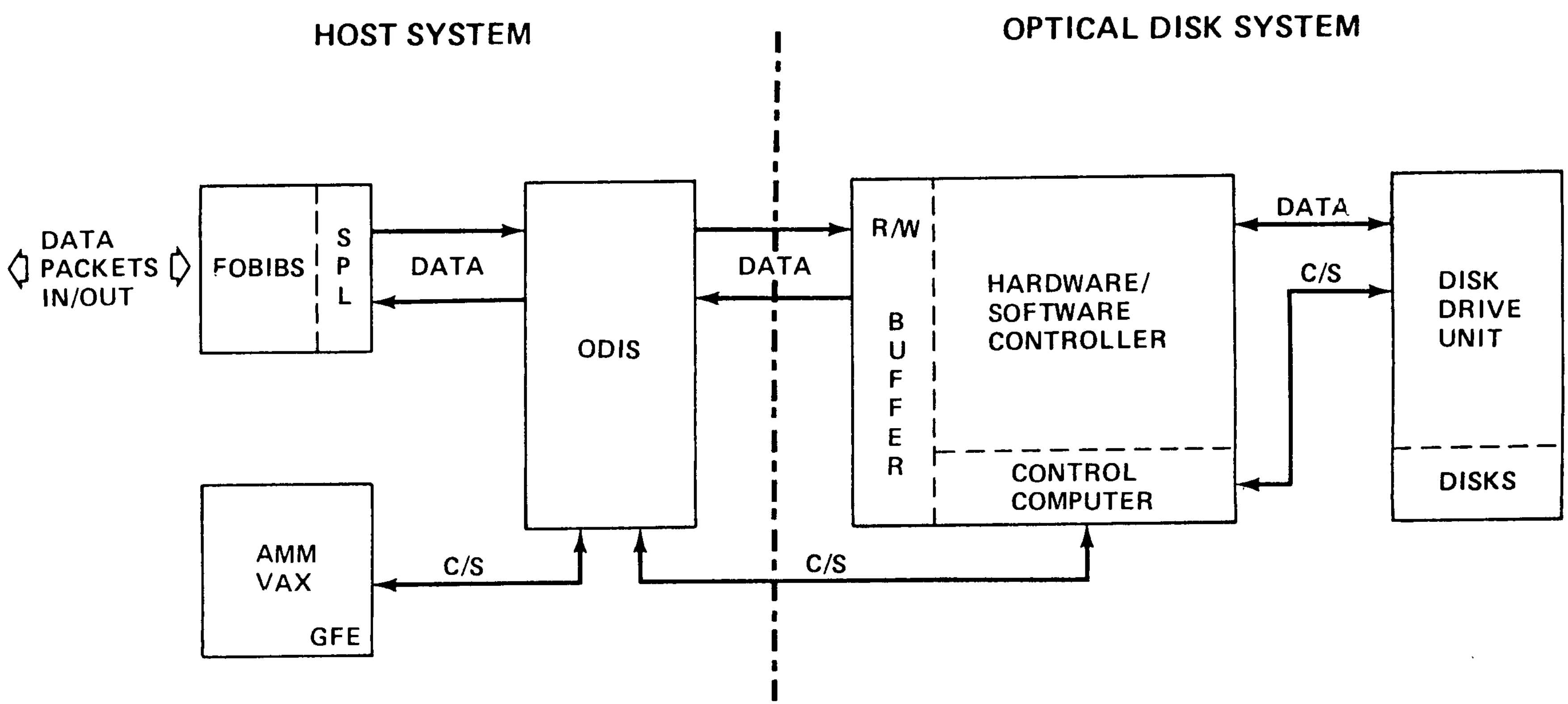

EB669
HARDWARE/SOFTWARE CONTROLLER
DATA PROCESSING UNIT (DPU)
DATA
DATA/
TEST
I/O
DATA
WRITE
BUFFER
WRITE
FORMATTER
DATA
DISC
CONTROL
SEQUENCER
READ
BUFFER
READ
FORMATTER
DATA
DATA
TO
DISC
DRIVE
UNIT
CONTROL
VAX
11/780
CONTROL
MASTER
CONTROL
PROCESSOR
SLAVE
PERIPHERAL
PROCESSOR
CONTROL PROCESSING HARDWARE (CPH)

EB670

OPTICAL DISK INTERFACE SYSTEM



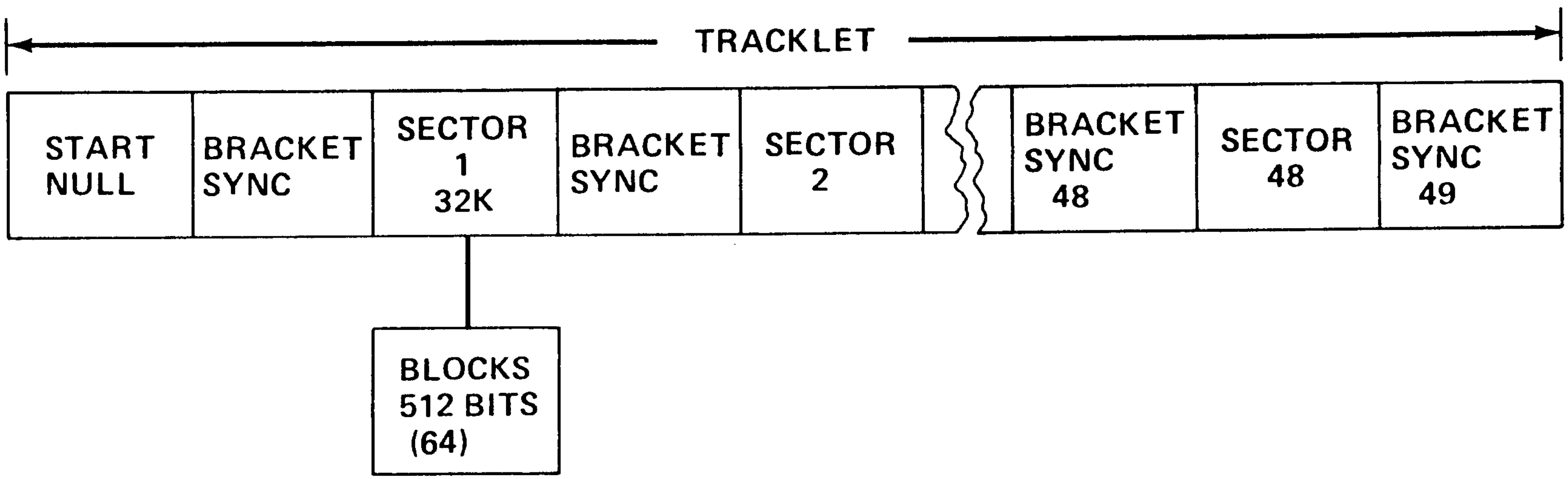
EB675

THREE LEVEL ERROR CHECK

- READ—AFTER WRITE FOR RECORDING
  - PERFORMED ON EACH INTERNAL BLOCK (512 BITS)
  - UP TO 40 REWRITES PERMITTED PER TRACK
- 3ϕ7 EDAC FOR OUTSIDE ENVELOP
  - CORRECTS FOR BURST ERROR
  - ENVELOP IS 32K BITS = 1 SECTOR
- 3ϕ7 EDAC FOR INSIDE ENVELOP
  - CORRECTS FOR RANDOM SINGLE BIT ERRORS
  - ENVELOP IS 512 BITS = 1 BLOCK

EB674

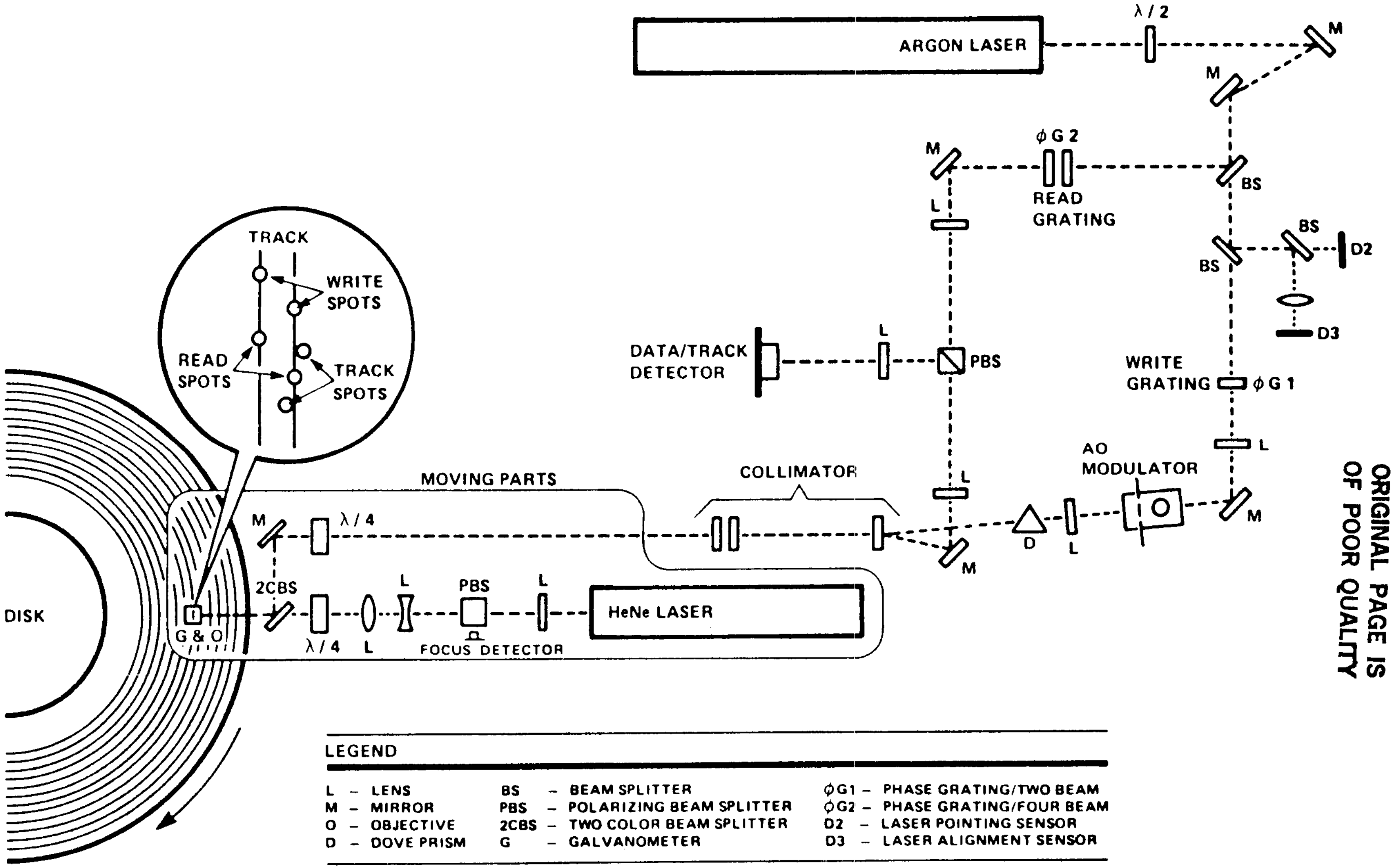
DATA FORMAT ON DISK



512 BIT = 1 BLOCK
64 BLOCKS = 1 SECTOR
48 SECTORS = 1 TRACKLET
2 TRACKLETS = 1 TRACK
22886 TRACKS = 1 DISK (7.8×10^{10})
125 DISK = $.975 \times 10^{13}$

EB671

OPTICS SCHEMATIC



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LEGEND

L – LENS	BS – BEAM SPLITTER	φG1 – PHASE GRATING/TWO BEAM
M – MIRROR	PBS – POLARIZING BEAM SPLITTER	φG2 – PHASE GRATING/FOUR BEAM
O – OBJECTIVE	2CBS – TWO COLOR BEAM SPLITTER	D2 – LASER POINTING SENSOR
D – DOVE PRISM	G – GALVANOMETER	D3 – LASER ALIGNMENT SENSOR

EB676

CAPACITY SUMMARY

	BITS	MAGNETIC DISK (300 M BYTE)	MAGNETIC TAPE (1600 BPI)	MAGNETIC TAPE (6250 BPI)
1 OPTICAL DISK	7.8×10^{10}	34	263	66
125 OPTICAL DISK ONLINE	$.975 \times 10^{13}$	4250	32,875	8250

PROGRESS/STATUS

- INSTALLATION, CHECKOUT, AND TESTING COMPLETE.
- OPTIMIZING OF SOFTWARE CONTINUES.
- HARDWARE CHANGES BEING MADE TO DISK DRIVE UNIT.
  - AUTOMATE BEAM ALIGNMENT WITH A SERVO.
- HIGH SPEED INTERFACE TO FIBER OPTIC BUS BEING DESIGNED FOR HIGH RATE INPUT
- LIMITED USE DUE TO UNAVAILABILITY OF DISK.

EB681

FUTURE OBJECTIVES

- INSTALL MULTIPLE TURNTABLES (MINIMUM OF TWO)
  - PROVIDE CONTINUOUS RECORDING
  - USER ACCESS TO PREVIOUSLY RECORDED DATA
- MODIFY SYSTEM TO PROVIDE CAPABILITY TO READ DATA SIMULTANEOUSLY FROM SAME DISK THAT IS BEING RECORDED ON
- REPLACE ARAGON LASER WITH LASER DIODE
- MODIFY TO RECORD/READ ERRASABLE MEDIA

N87-29157

P.20

Abstract

Network control (or network management) functions are essential for efficient and reliable operation of a network. Some control functions are currently included as part of the OSI (Open Systems Interconnection) model. For local area networks it is widely recognized that there is a need for additional control functions, including fault isolation functions, monitoring functions, and configuration functions. These functions can be implemented in either a central or a distributed manner. The FDDI (Fiber Distributed Data Interface) Medium Access Control and Station Management protocols provide an example of a distributed implementation.

Network Reliability

Marjory J. Johnson

Research Institute
for Advanced Computer Science
NASA Ames Research Center

Outline

- Meaning of network reliability
- Current approach to problem
- Additional issues to address
- Implementation alternatives
- Issues for study

State of local area network technology

- Past –
  Mechanics of communication emphasized

- Present –
  Need for network control recognized

- Space Station –
  Requires high degree of reliability

Meaning of Reliability

- Wide area networks –

  Degree of connectivity, i.e., availability of alternate routing

- Local area networks –

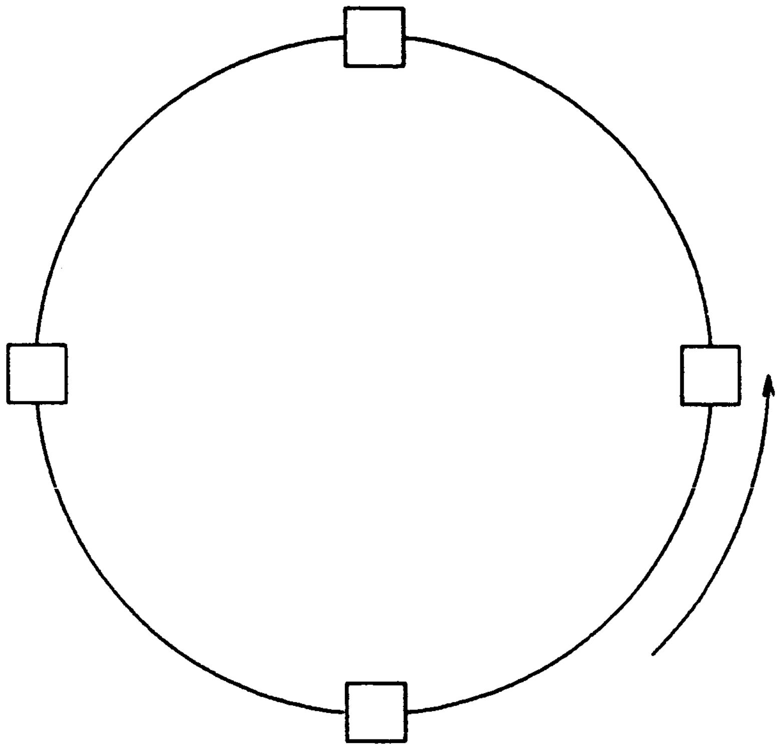
  Ensuring that a single error will not cause failure of the entire network

  Providing for recovery from errors without significant degradation of performance

General Reliability Concerns for LANs

- Cable vulnerability
- Jabbering transmitter
- Failure isolation
- Bit synchronization
- Protocol-related problems

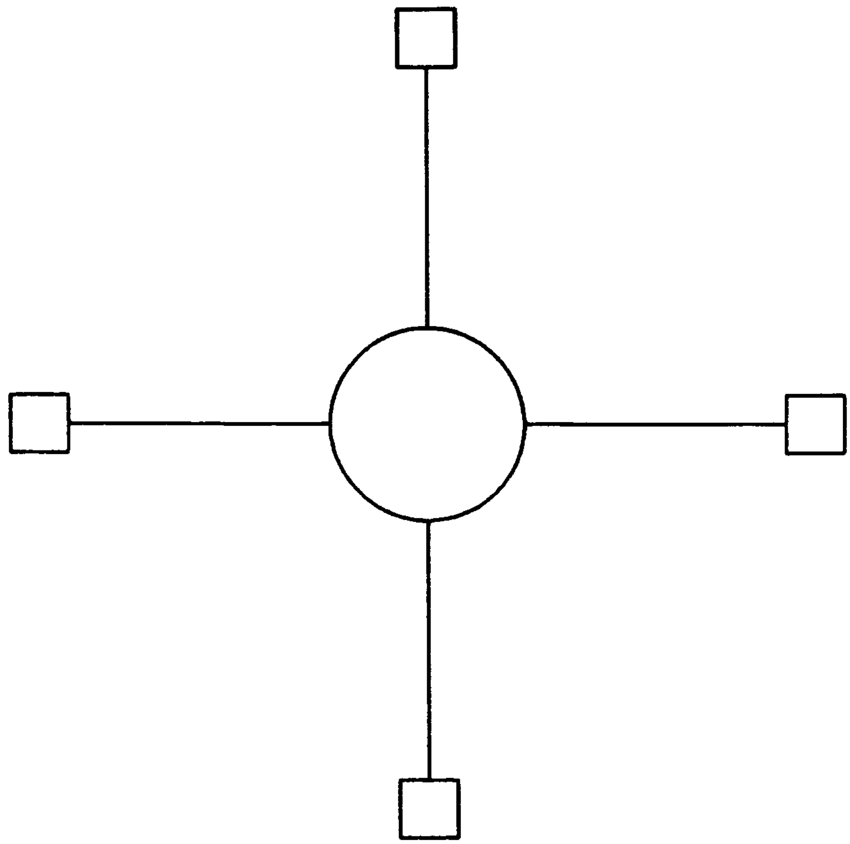
Token Ring



Reliability concerns

- Break in physical path
- Token–related problems
    - Lost token
    - Duplicate tokens
    - Token recovery

Star Topology



Reliability concerns

- Vulnerability of star node
- Complexity of star node
- Coordinating time–slots
- Station insertion or removal

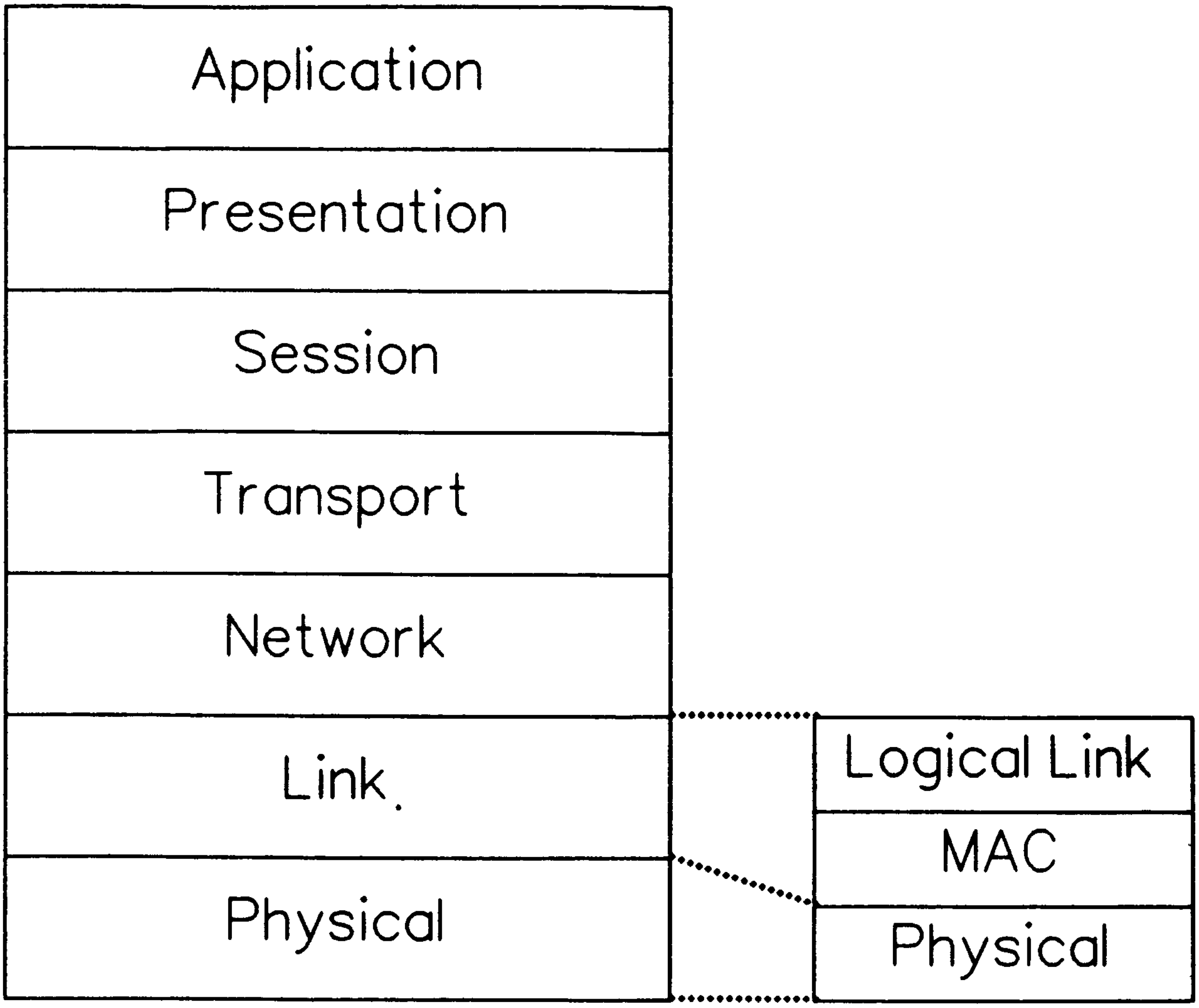
Layers of OSI Model

Application
Presentation
Session
Transport
Network
Link
Physical

OSI Control Functions

- Link Layer
  - Flow control
  - Error control
  - Acknowledgement
- Network Layer
  - Virtual circuit service
  - Datagram service
  - Congestion control
- Transport Layer
  - Buffer control
  - Connection management
  - End–to–end error recovery and flow control
- Application Layer
  - Network management

Layers of OSI Model for Local Area Networks



Local Area Network Control

- Fault isolation
  - Monitor network to detect faults
  - Isolate fault to single component
  - Fault correction
- Monitoring functions
  - Performance measurement
  - Performance analysis
  - Artificial traffic generation
- Configuration functions
  - Directory management
  - Set station parameters
  - Station insertion and removal
  - Station reset

Statistics to gather

- number of packets
- number of packets by source
- number of packets by destination
- number of data packets
- number of control packets
- packet size
- packet delay
- number of retransmissions
- number of collisions
- number of packets received in error

Data analysis

- Distribution of traffic
- Excessive collisions?
- Excessive retransmissions?
- Excessive packet delay?
- Success of station in transmitting packets
- Maximum capacity of channel
- Effect of traffic load on performance

Artificial traffic generation

- Test network in laboratory
- Indicate existence of potential problems
- Indicate efficiency of system
- Plan for future growth

Implementation alternatives

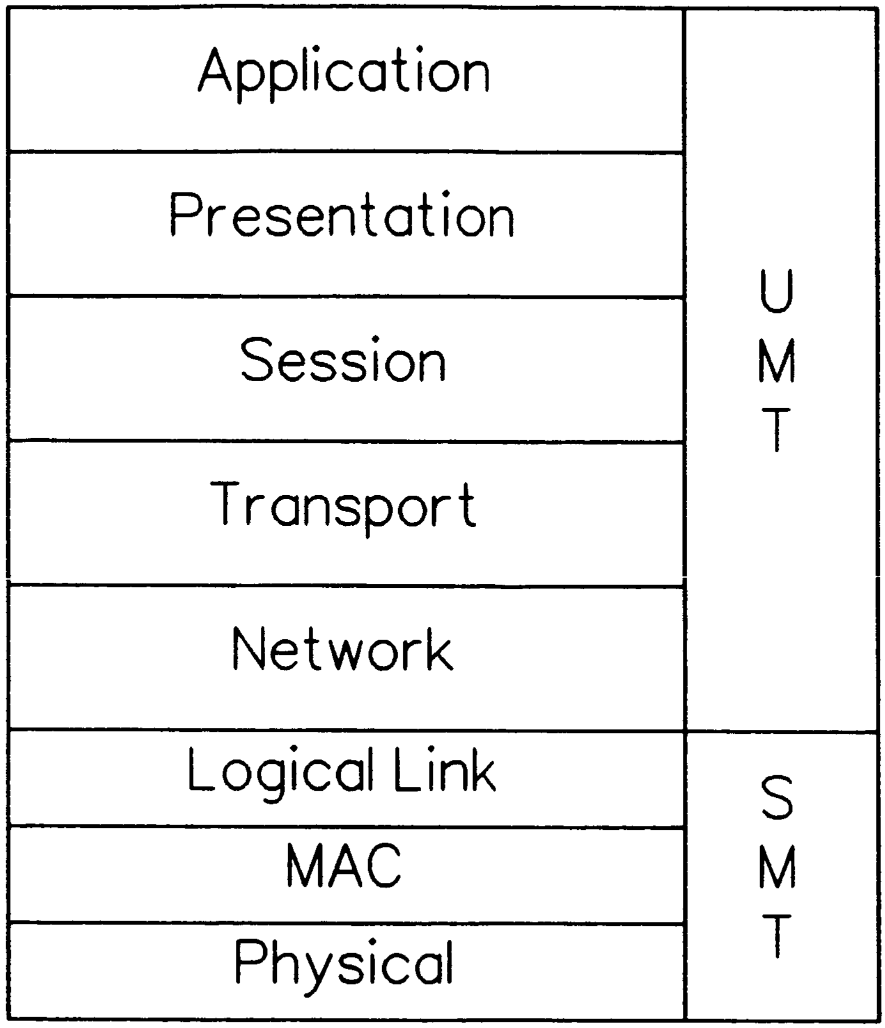
Central

- Network Control Center
- NBS "measurement center"

Distributed

- Separate network control layer
- Implementing control functions in each layer

FDDI Network Control



SMT = Station Management
UMT = Upper Management

FDDI Implementation of control functions

- Fault isolation functions
  - Timers
  - Claim token recovery process
  - Beacon frame
- Configuration functions
  - Optical station bypass
  - Redundant channel
  - Station Management functions
    - Station reset
    - Insertion of station
    - Timer alignment

- Monitoring functions
  - Status bits
  - Station flags
    - Error detected
    - Address recognized
    - Frame copied
  - Station counters
    - Frames received
    - Timer expirations
  - Interface to Station Management

Open Issues

- Identify proper control functions to assign to upper layers of the OSI model
- Determine effect on network performance and network reliability of
  - Buffer management
  - Acknowledgement schemes
  - Retransmission schemes
  - Multi–layer protocol structure
- Determine how to automate control functions

FAULT-TOLERANT SOFTWARE EXPERIMENT OBJECTIVES AND STATUS

Dave E. Eckhardt, Jr.
NASA Langley Research Center

NASA
Computer Science / Data Systems
Technical Symposium

April 16–18, 1985

N87-29158

P-7

BACKGROUND

- Redundancy is an established principle for dealing with hardware faults.

- Software redundancy (modeled after hardware NMR and stand-by sparing techniques) has been advocated as a method to cope with residual software faults.

- Current use of redundant software includes:
  - Airbus Industries A310 slat and flap control
  - Swedish state railroads traffic control system
  - Boeing 737-300 critical flight control functions
  - Boeing 757 yaw damper and stabilizer trim systems
  - Atomic Energy of Canada nuclear reactor shutdown system
  - NASA Space Shuttle mission critical functions

OBSERVATIONS*

- No examples found where last phase of fault-tolerance, fault treatment, was an integral part of system.

- Trend in which regulatory agencies recommending redundant software to improve reliability.

- Empirical data needed to quantitatively evaluate performance has not been kept. Statements of improved reliability and cost trade-offs could not be made.

- No evidence that software redundancy degraded reliability.

- Instances of faults detected during code testing and faults in specifications as a result of redundant software.

*Study of Fault-tolerant software technology
NASA Contractor Report 172385

MAJOR ISSUES

RELIABILITY

- Little empirical data to assess reliability
- Independence assumption of current reliability models is questionable
- Prevalance of coincident errors in "independent" versions is unknown
- Cost of reliability gains is unknown

RELATION TO HARDWARE FAULT–TOLERANCE

- Layered or integrated hardware/software fault–tolerance
- Required hardware, operating system support for effective implementations

APPLICABILITY

- No examples of fault–tolerant operating systems
- Closed–loop systems present stability problems when certain fault–tolerant techniques introduced

EXPERIMENT OBJECTIVES

- Develop analytical methods to evaluate the general strategy of software redundancy to improve reliability.

- Gather empirical data to characterize fault distributions of coincident errors.

  - realistic application 3–5 mm effort
  - well tested, reliable software
  - software engineering practices
  - quality programmers

- Characterize coincident fault types and suggest methods to reduce their intensity coefficient.
  (speculate these are the residual faults, thus this effort should benefit software engineering in general)

CURRENT STATUS

- Grants to participating universities in place (UVA, UCLA, U Illinois, NC State)
- Hiring of programmers nearing completion
- Application selected
- Probabilistic framework for analysing multi-version software in the presense of coincident errors developed
- Definition of experiment protocol and development environment nearing completion

FUTURE ACTIVITIES

- Software specifications (Apr 10 - June 1)
- Software development (June 1 - Aug 15)
- Extensive life testing (Aug 15 ...)
- Reliability analysis

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P.18

UVA DEPARTMENT OF COMPUTER SCIENCE

PROGRAMMING FAULT-TOLERANT DISTRIBUTED SYSTEMS IN Ada

Susan J. Voigt

Computer Science And Applications Branch
Langley Research Center

For Presentation At
The Computer Science/Data Systems Technical Symposium
Leesburg, Virginia

April 18, 1985

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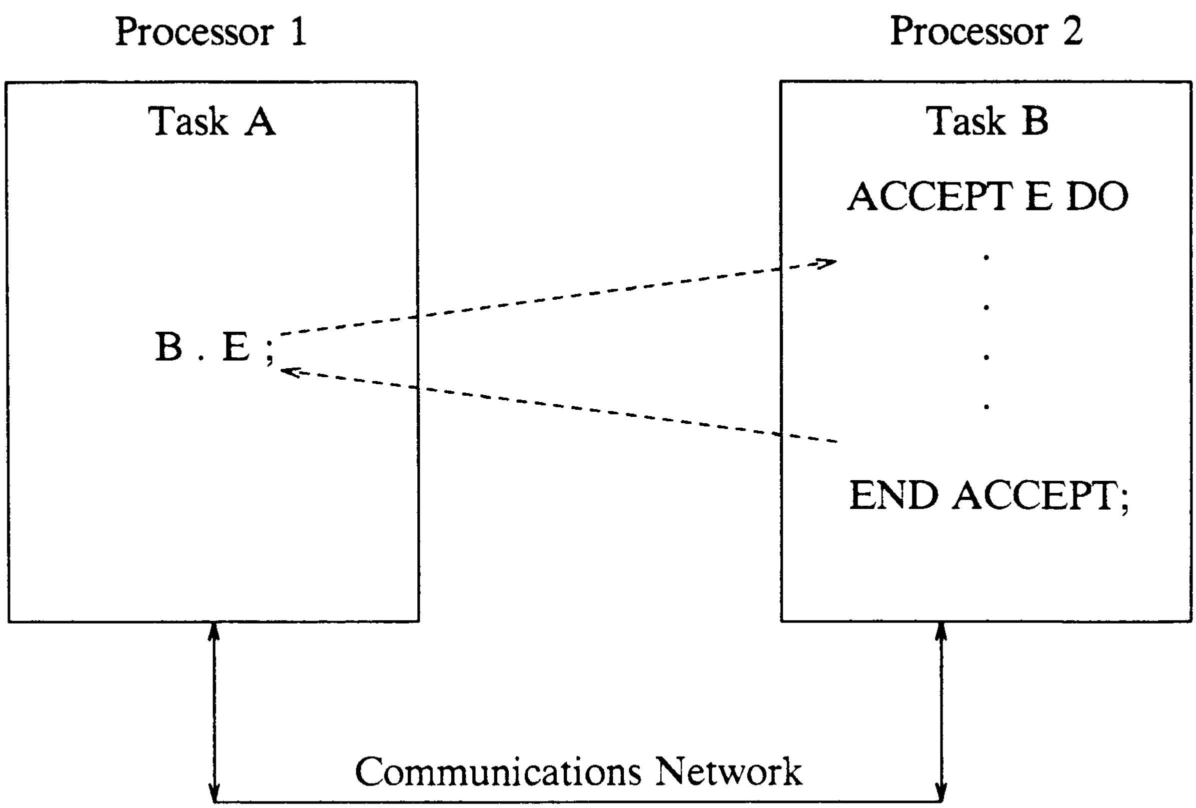
PROJECT GOALS

- Examine Use And Implementation Of Ada On Distributed Systems
- Programming Of Systems With "Fail-Stop" Components
- Analyze Tolerance To Loss Of Processors
- Propose Solutions To Language Inadequacies
- Implement These Solutions
- Perform Validation Experiments
- Suggest Long-Term Changes To Ada

WHY Ada ON DISTRIBUTED SYSTEMS?

- Ada Will Be Used Extensively In Embedded Systems
- Embedded Systems Will Be Distributed
- Many Applications Will Be Crucial
  - — Spacecraft Systems
  - — Aircraft Systems
  - — Industrial Process Control
- Distributed Systems Should Support Graceful Degradation
  - — Partial Power Failure
  - — Physical Damage
  - — Component Failure
- Ada Permits Distributed Targets Explicitly

Ada RENDEZVOUS



- Task A Suspended If Processor 2 Fails During ACCEPT

Ada DIFFICULTIES

- Language Elements That Cause Difficulty:
  - — All Forms Of Rendezvous
  - -- Shared Variables
  - — Task Elaboration And Termination
  - — Loss Of Context
  - — Distribution Control
  - — Processor Loss - Detection And Signaling
- Complete Lack Of Distribution Semantics
- Complete Lack Of Failure Semantics

SOLUTIONS

- Short Term:
  - — Define Simple Distribution Semantics
    - What Can Be Distributed
    - Where It Can Be Distributed
    - Control Of This Distribution
    - Necessary Restrictions On Program Structure
  - — Define Failure Semantics As Equivalent To "ABORT"
- Long Term:
  - — Complete Redefinition Of Tasking Semantics
  - — Partial Replacement Of Tasking Syntax
  - — Language Support For Distributed Systems Using Fail-Stop Components

STATUS OF SOLUTIONS

- Language Review Complete
- Short Term Solution:
  - Distribution Semantics Complete
  - Failure Semantics Complete
  - Implementation Design Complete
  - Implementation Complete And Under Test
  - Realistic NASA Application Required For Evaluation Of All The Ideas
- Long Term:
  - Several Proposals Being Examined
  - Radical Changes To Ada Required
  - U.Va's Ada-2 Design Expected Soon

OTHER ISSUES IN DISTRIBUTED SYSTEMS

- Concurrency Implies Nondeterminism
- Difficulties With "What If" Questions Of Language Semantics
- Difficulties With "What If" Questions Of Fault-Tolerance Strategy
- Require "Complete" Demonstration Of Fault Tolerance
- Systematic, Repeatable Experiments

TESTBED REQUIREMENTS

- Model Arbitrary Physical Architectures
- Represent Any Logical Organization
- Provide Parallel Execution (The Illusion At Least)
- Control Interprocessor Communication
- Control Process Execution
- Fail And Restart Processors At Well-Defined Points
- Maintain Time Correctly
- Provide Monitoring Facilities

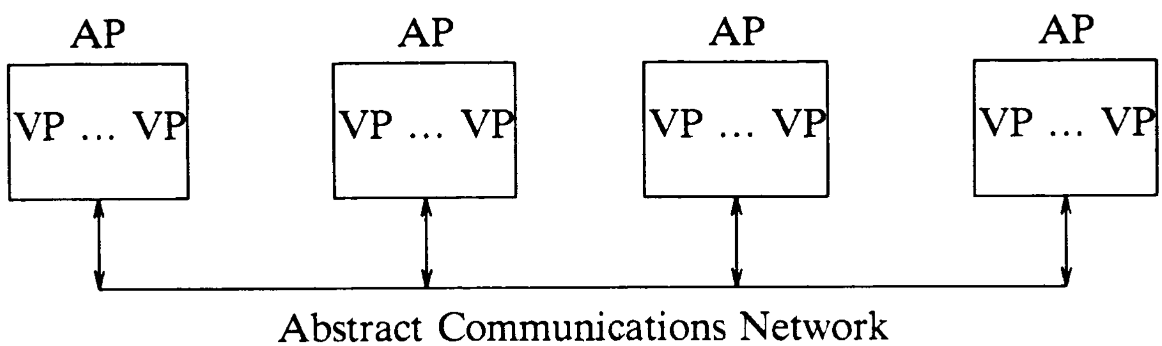
VIRTUAL PROCESSORS

- Key Component Of The Testbed
- Literally Ada "Virtual Machines"
- One Virtual Processor For Each Ada Task In A Program
- Designed To "Implement" Ada Tasking And Exception Handling
- Several Different "Memories" - Whatever Is Convenient
- "Hardware" Implemented Entry Queues
- "Rendezvous" And Similar Instructions
- Implemented By Simulation

ABSTRACT PROCESSORS

- Correspond To "Real" Equipment Required By Experimenter
- Each Abstract Processor Implements Any Number Of Virtual Processors
- Abstract Processors Are "Ideal" Also - E.G. Suspended, Failed, Etc
- Abstract Processors Communicate Via An Abstract Communications System
- Testbed Supports An Arbitrary Number Of Abstract Processors

EXPERIMENTAL STRUCTURE

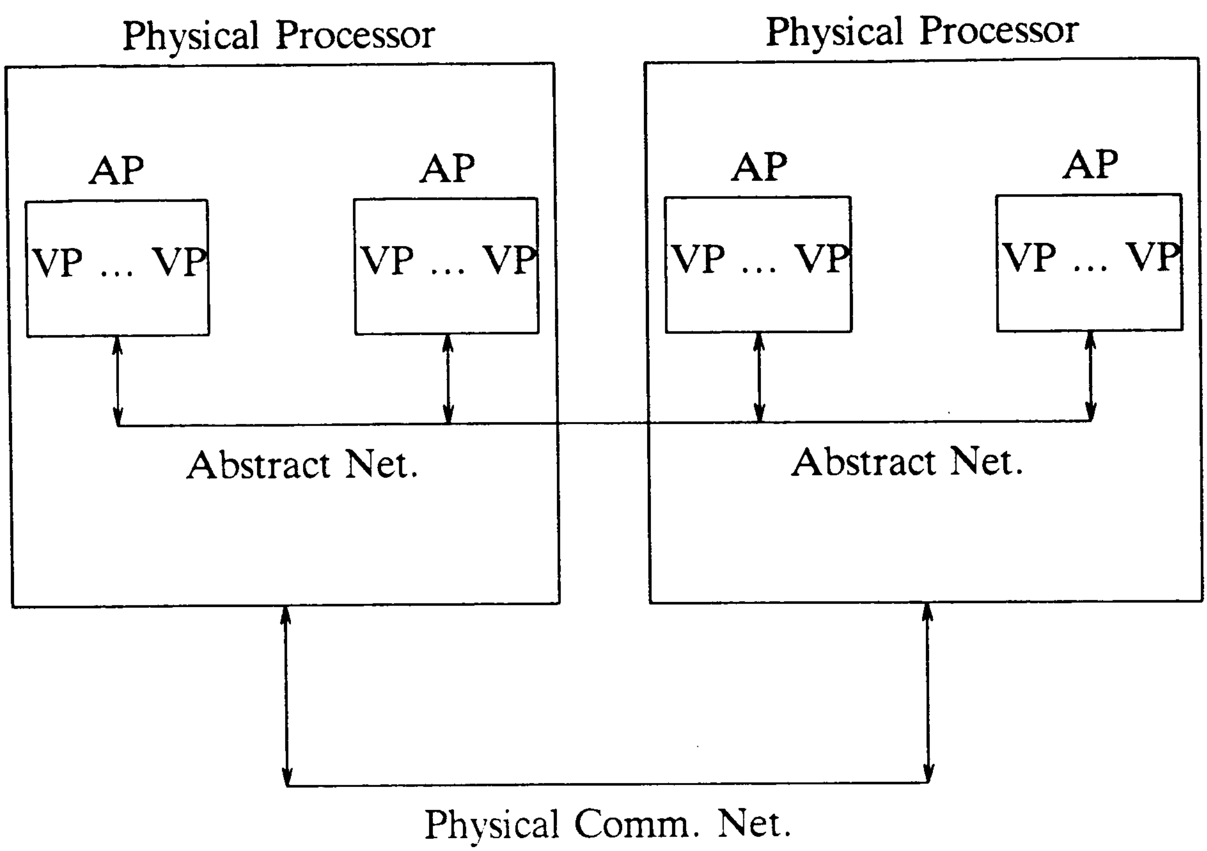


- View Seen By Experimenter
- AP's Represent Ultimate Target He Has In Mind

PHYSICAL PROCESSORS

- Correspond To "Actual" Equipment Available To Experimenter
- Each Physical Processor Implements Any Number Of Abstract Processors
- Physical Processors Are "Real"
- Physical Processors Communicate Via A "Real" Communications System
- Single Abstract Processor Can Run On Each Physical Processor

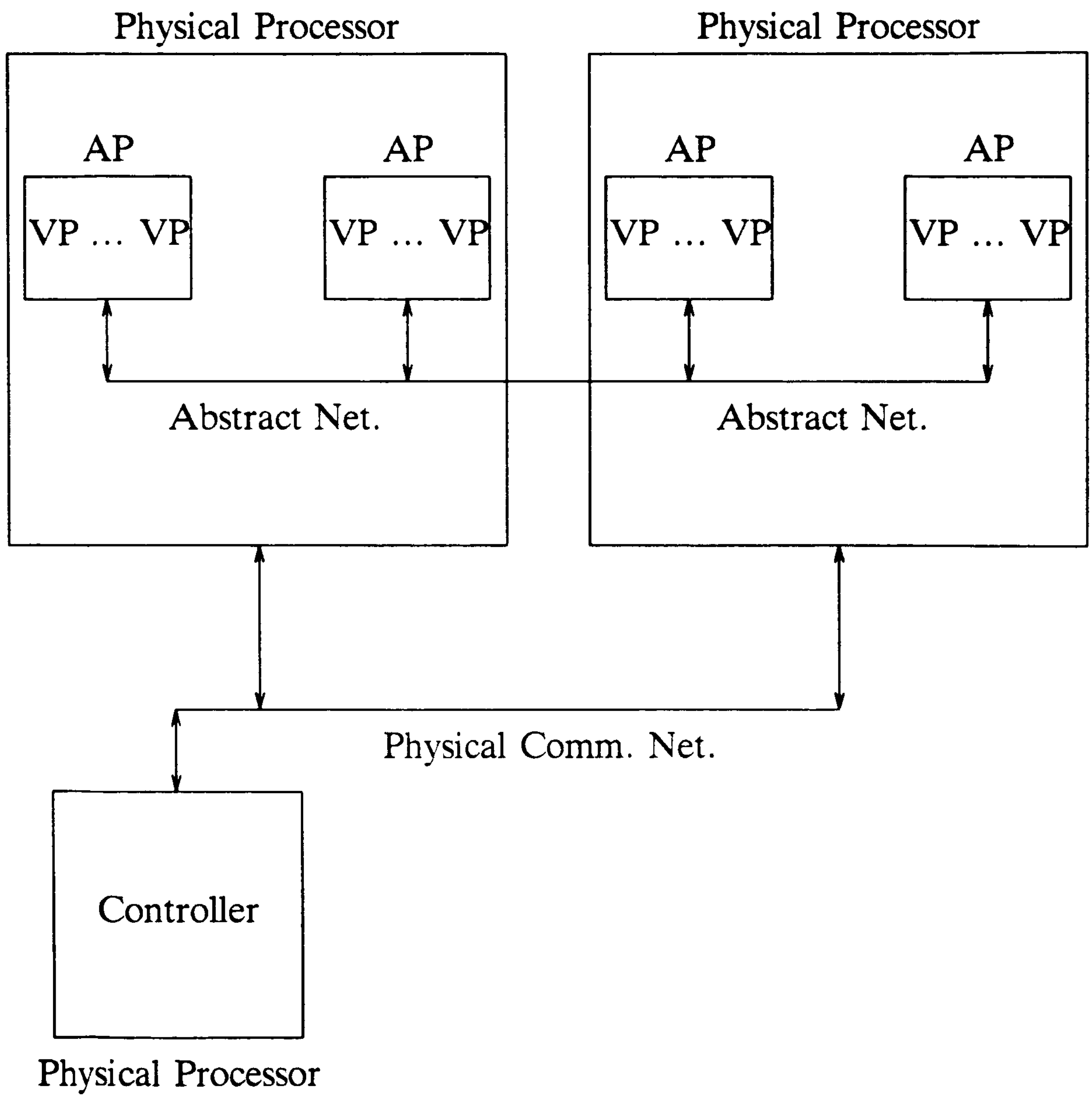
TESTBED STRUCTURE



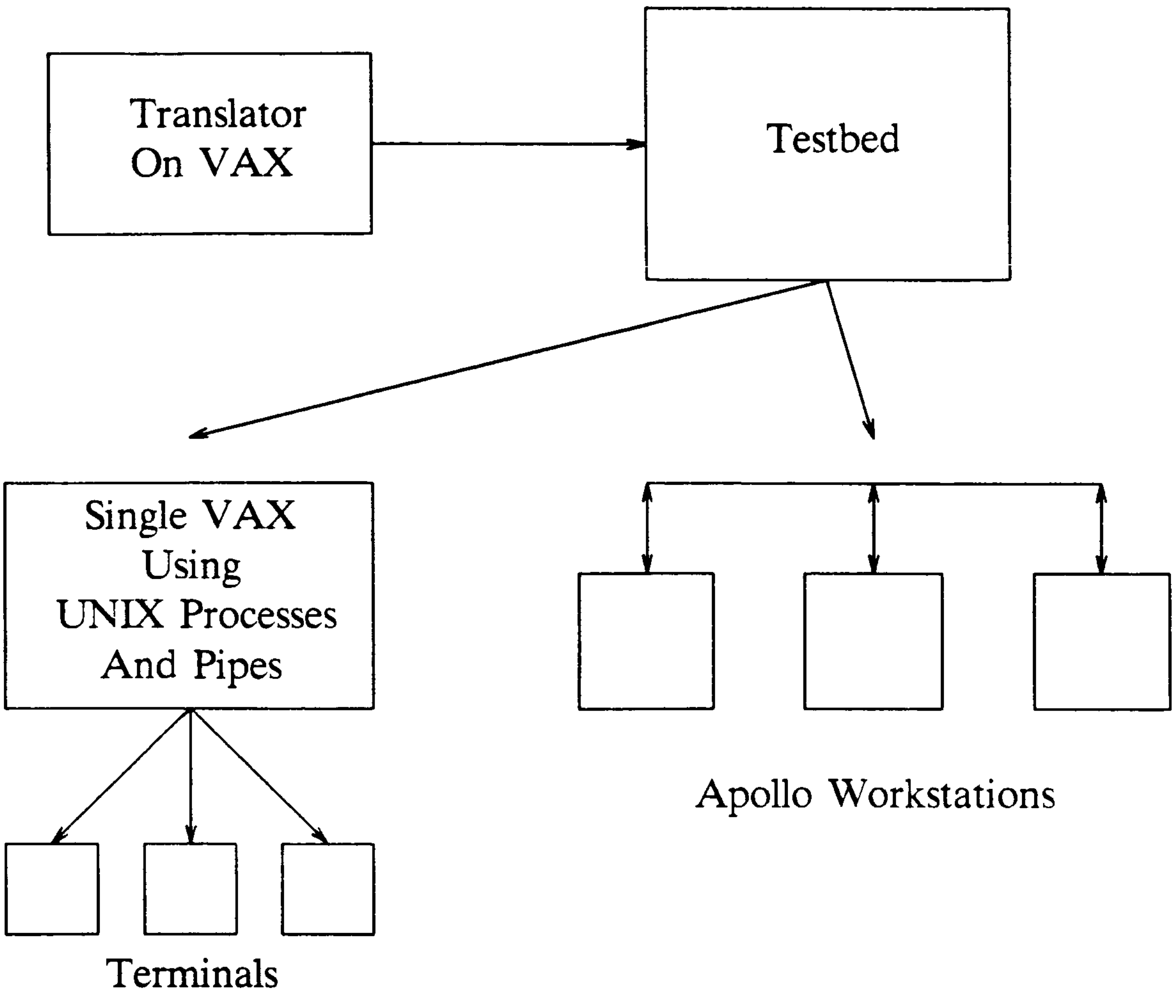
CONTROLLER

- Start, Stop, Single-Step Ada Tasks
- Control Communication At The Message Level
- Manage Breakpoints On A Per-Task Basis
- Arrange Failure Of Abstract Processors
- Collect And Display Information For Experimenter

TESTBED CONTROL



IMPLEMENTATION



CONCLUSIONS

- ANSI Ada Does Not Support Processor Failures Well
- ANSI Ada Can Cope Given:
  - — Minor Semantic Enhancements
  - — No Syntax Changes
  - — Major Additions To Execution-Time System
- Demonstration Implementation Being Developed At The University Of Virginia
  - — A Feasibility Study
  - — Not Suitable For Production Use
- Realistic Application Needed For Evaluation Purposes
- Ideal Solution Requires Extensive Language Changes

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FIBER OPTICS COMMON TRANSCEIVER MODULE

Herbert D. Hendricks

NASA Langley Research Center

Long Term Objectives:	Develop space qualified fiber optics transceiver for information networks application in Space Station. Advance the technology to increase the system data handling capability, reduce the overall device size and improve efficiency and sensitivity.
Importance of Problem:	Fiber optics information networks provide a means to achieve a high data rate communication system that is evolutionary and expandable for use on the Space Station. A space/military qualified approach to the problem will help advance the technology development and make more refined and advanced communications system available earlier.

FIBER OPTICS COMMON TRANSCEIVER MODULE

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Related R & D: Comments related to other R & D in this area has been obtained from AGED"C" reviews, Tri-Service Working Group on Fiber Optics, Published Literature and Private Communications.

Hybrid Fiber Optics Transceivers: Commerically available devices are available from a few kiloBits to 500-700 MegaBits that are designed around discrete devices and combinations of discrete devices and hybrid integrated devices. High speed transceivers tend to use more integrted devices such as pin-FET preamplifiers, amplifiers and comparators. GaAs FET laser driver circuits are coming into greater use. This also includes the hybrid integration of the laser current mirror drive circuit. DOD, U.S.Army, has a military qualified 50 MBit transceiver module.

Monolithic Fiber Optics Transceiver: Currently DARPA is funding Rockwell International and TRW for the integration of semiconductor lasers and photodetectors with GaAs FET technology for high speed transceivers for fiber optics and microprocessor communications.

DOD is also funding some monolithic pin-FET preamplifier development in InGaAsP/InGaAS/InP which was formerly funded by NASA. Objectives of the program also encompasses a transmitter development effort.

Japan has demonstrated a number of monolithic approaches for a pin-FET preamplifier and a laser FET in InGaAs and AlGaAs

FIBER OPTICS COMMON TRANSCEIVER MODULE

Technical Approach:	The technical approach centers around past in-house tasks in the development of hybrid fiber optics transceivers, coordination of transceiver development with DOD and finally a RADC study of transceiver requirements for the Air Force.
Fiber Optics Hybrid Transceiver:	The current approach is to build onto a RADC common transceiver module contract which is currently dircted toward a 200 MBits transceiver within one year. NASA also prevailed to have an added breadboard development of a 1 GBit design. GaAs foundry services are being followed along with commerical development of hybrid integrated transceiver devices. A 3 GBit front end laser driver and photodetector preamplifier is being pursued in-house using available GaAs GigaBit technology.
Monolithic Transceiver:	Discussions are being carried on with a number of DOD offices about the next generation transceiver designs. Discussions center around both AlGaAs and InGaAsP material/device systems.

FIBER OPTICS COMMON TRANSCEIVER MODULE

Technical Results and Accomplishments

Hybrid Transceivers

Demonstrated an in house version utilizing a hybrid receiver approach consisting of 1) an integrated pin-FET transimpedance preamplifier, 2) Avantek amplifiers, and 3) high speed ECL comparators. Transmitter design utilized a GaAs-FET current mirror and bias circuitry, Tau-Tron drivers and photodiode feedback and T.E. cooler control circuitry. Device performs at 500 MBits at 1 milliwatt power output, -35 dB sensitivity and with 10^{-10} bit error rate in fiber optics networks.

Designed a 3 GBit transmitter and receiver front end based on GaAs FET GigaBit Logic Devices. Investigated Tektronix CAD GaAs FET design based Daisy Systems and corresponding foundry services.

Currently have a joint contractural effort with RADC for the development of a 200 Mbit/sec military qualified transceiver and a breadboard study of a 1 GBit/sec transceiver.

Monolithic Transceiver

Tracking DOD R & D efforts and Japanese efforts while looking for supporting funds.

Progress towards planned milestones on schedule.

FIBER OPTICS COMMON TRANSCEIVER MODULE

HOW CURRENT RESULTS AND ACCOMPLISHMENTS WILL ENHANCE NASA CAPABILITY IN COMPUTER SCIENCE AND DATA SYSTEMS

Current advancements in commerical and military qualified device/component/transmitter/receiver technology point toward the acceptance of fiber optics in communications, computer and data systems. This task will be the implementation of technology to provide a space qualified transceiver for use on Space Station. With the complimentary funding from RADC/AF this should supply a much needed transceiver for use on Space Station with relative little NASA funds and in a short time frame.

A greater advancement could be made by utilizing GaAs FET technology to reduce the ECL power consumption and improve the overall electronic/optical system thermal load while increasing the ability to transfer data at higher speed with greater efficiency.

GaAs mesFET and GaAs HEMT technology with both depletion and enhancement devices will provide the high speed parallel processing capability of the future.

FIBER OPTICS COMMON TRANSCEIVER MODULE

MAJOR MILESTONES

Demonstrate military qualified transceiver - 4/86

Demonstrate 1 GBit breadboard transceiver design -4/86

Demonstrate Space Qualified Transceiver - 6/87

Demonstrate greater than 1 GBit transceiver - 6/88

RESOURCE REQUIREMENTS	85	86	87	88	89
($k)	0	200	200	400	400
(MY)	0	.1	.1	.2	.2

FIBER OPTICS COMMON TRANSCEIVER MODULE

ISSUES: Funding for GaAs-FET Transceiver
Space Qualifications for Space Station
Upper Limit Data Rate Requirement

COMMENTS: All programs coordinated with DOD Tri-Service Committee on Fiber Optics

 N87-29161

SPACE STATION FOCUSED TECHNOLOGY

"ELECTRONIC CONTROL/DISPLAY INTERFACE TECHNOLOGY"

p.26

R. V. Parrish, A. M. Busquets,
R. F. Murray, J. J. Hatfield
NASA-Langley Research Center

The objective of this effort is to achieve, through an orderly process of assessment, analysis, design, development and test, a representation of an advanced workstation for inclusion in the Space Station Data Management Test Bed. The workstation will use presently available technological elements and will be adaptive to future evolutionary technologies, advanced architectures, and enhanced software. The effort will be nurtured by the advanced control/display and human factors technology emanating (past, present, and future) from the NASA Aeronautical R&T Base program in Crew Station Technology, which provides a firm basis for consolidating, automating, and integrating the interface between man/machine.

Promising technologies to be considered for inclusion in the workstation are: high-performance all-rastergraphic pictorial display generation, advanced display media (including flat panel displays), interactive multifunction controls (including touch and voice), advanced workstation processors, and interactive video disc hardwares, as well as the software base, methodologies, and techniques for their integration into advanced workstation concepts. Image management technologies for the storage, retrieval, and routing of computer-generated data, live imagery, video disc imagery/data, and combinations of these in windowed displays will be emphasized.

The program plan (i.e., to achieve the objectives of providing innovative and flexible user options which support clean, uncluttered workstations that fulfill space station requirements) consists of three phases. The initial phase provides for the determination of the control/display information and functional requirements to furnish such capabilities as systems monitoring/control, office automation functions, resource management, and data base management, as well as a survey of the available devices and systems technologies (display generators, workstation processors, display medias, multifunction controls, etc.). The second phase deals with the evaluation, through an interim workstation, of the architectural options, the implementation strategies, and the space station applications for technology demonstration that will be incorporated into the final workstation. The final phase consists of assembling the deliverable workstation and interfacing it to the Data Management Test Bed at Johnson Space Flight Center.

In summary, this effort will produce a representative workstation for the Space Station Data Management Test Bed that provides man/machine interface design options for consolidating, automating, and integrating the space station workstation, and hardware/software technology demonstrations of space station applications. The workstation will emphasize the technologies of advanced graphics engines, advanced display/control medias, image management techniques, multifunction controls, and video disc utilizations. In addition, the effort will contribute to the overall knowledge base of man/machine interface design methodologies.

COMPUTER SCIENCES AND DATA SYSTEMS
TECHNICAL SYMPOSIUM

APRIL 18, 1985

LEESBURG, VIRGINIA

SPACE STATION FOCUSED TECHNOLOGY

"ELECTRONIC CONTROL/DISPLAY INTERFACE TECHNOLOGY"

AUTHORS

R. PARRISH, R. MURRAY
A. BUSQUETS, J. HATFIELD

SPEAKER

J. HATFIELD

NASA-LANGLEY RESEARCH CENTER

PRESENTATION CONTENTS

- o R & T AVIONICS PROGRAM BACKGROUND
- o SPACE STATION ELECTRONIC CONTROL/DISPLAY INTERFACE TECHNOLOGY EFFORT
  - OBJECTIVES/BENEFITS
  - PROGRAM PLAN
- o CURRENT STATUS
- o RESOURCES
- o SUMMARY

NASA
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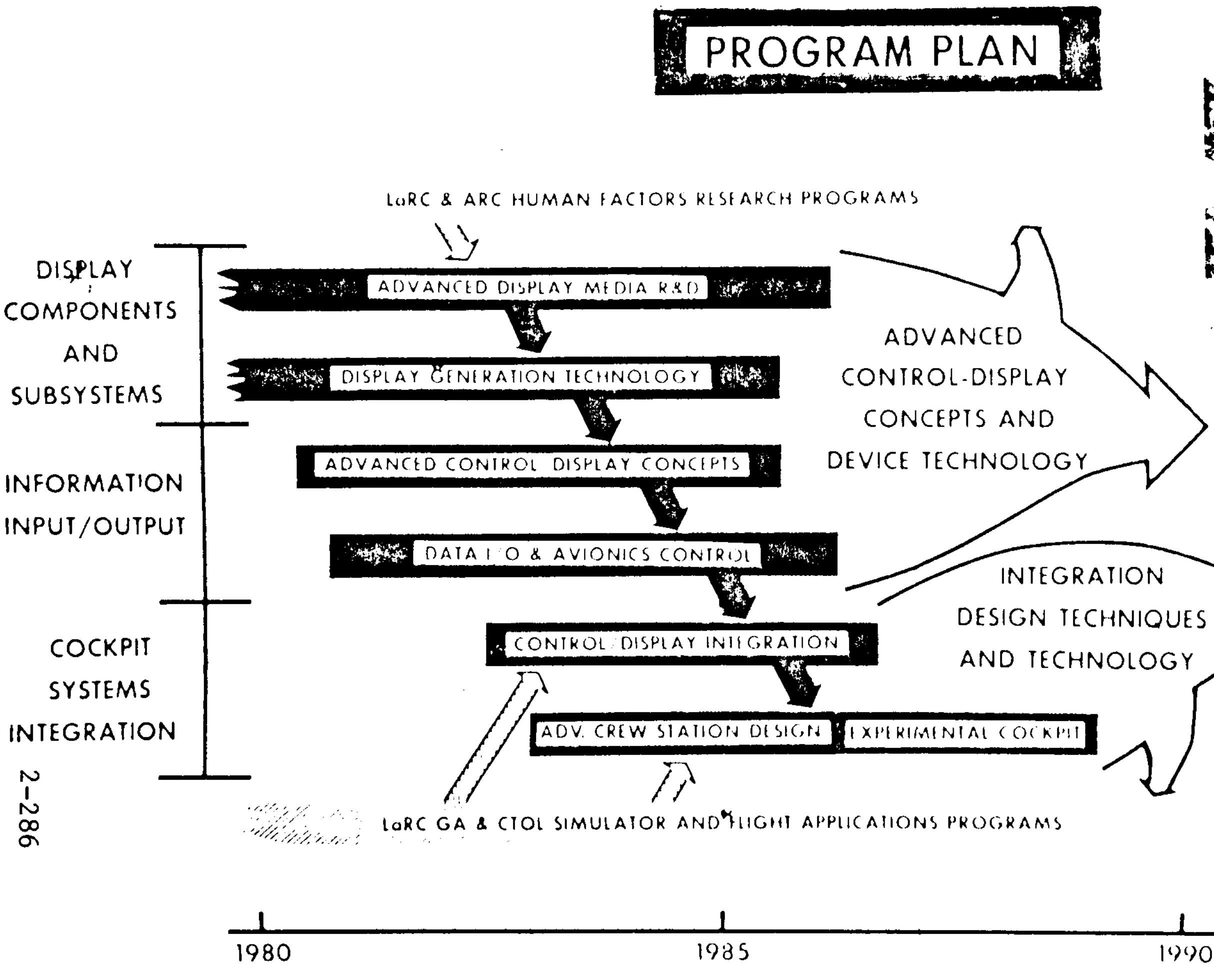
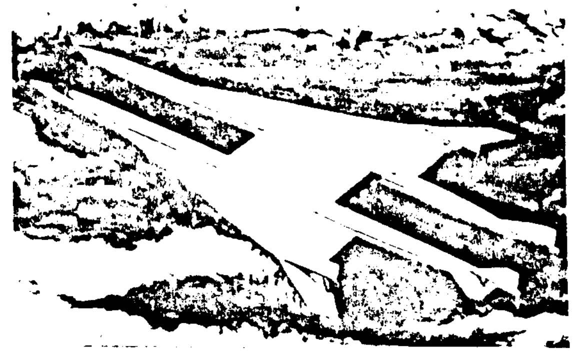
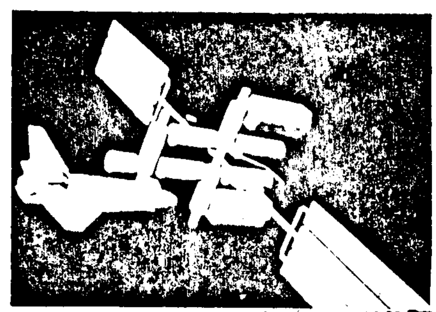
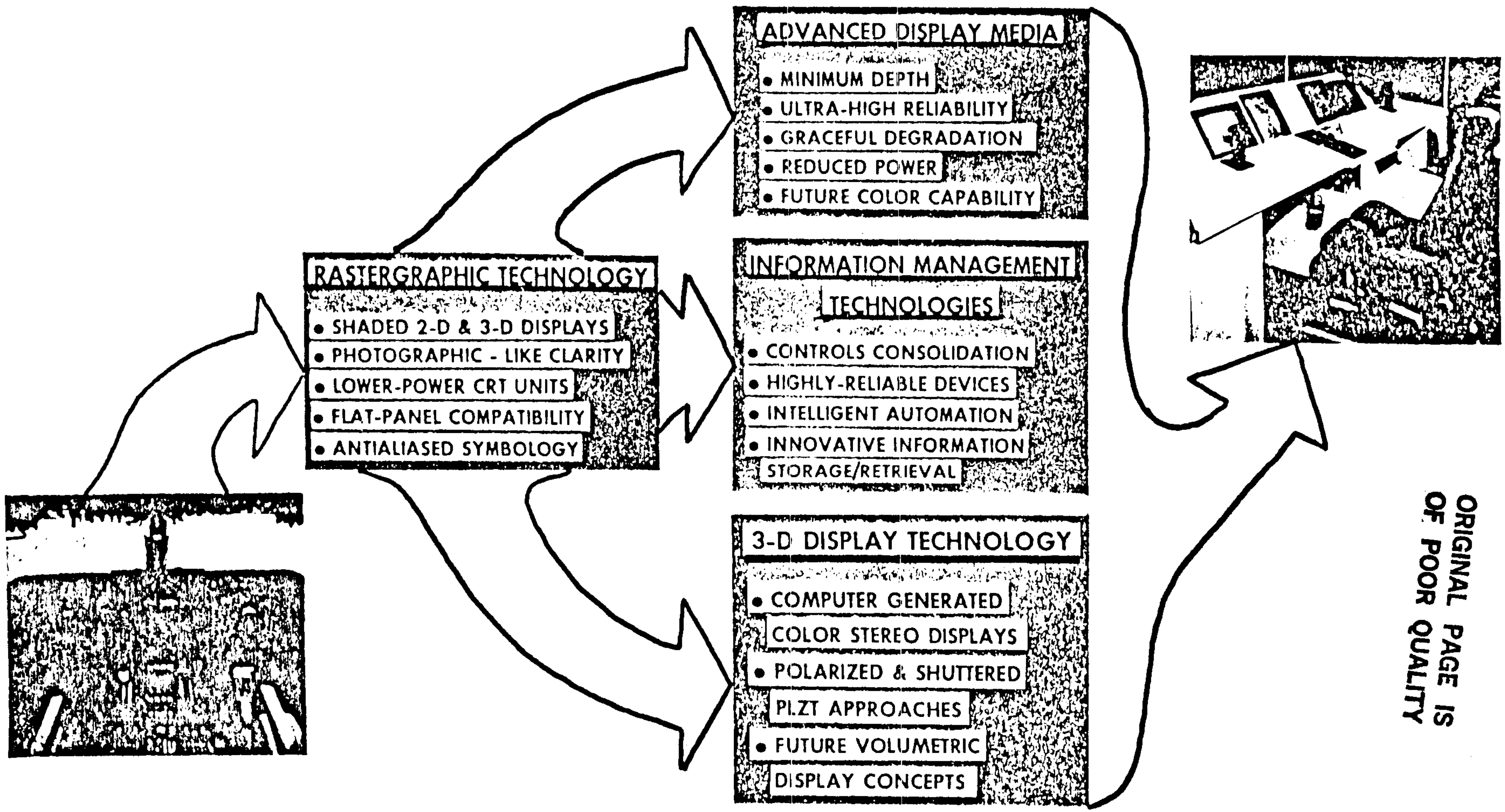
ADVANCED NAVIGATION, GUIDANCE, AND CONTROL PROGRAM
CREW STATION ELECTRONICS TECHNOLOGY ELEMENT







RESEARCH THRUSTS IN CREW STATION TECHNOLOGY



AREAS OF CONTROL/DISPLAY R&D

GENERIC SPACE
WORKSTATION REQUIREMENTS

INTERACTIVE
WORKSTATIONS FOR
MONITORING & CONTROL
SPACE STATION

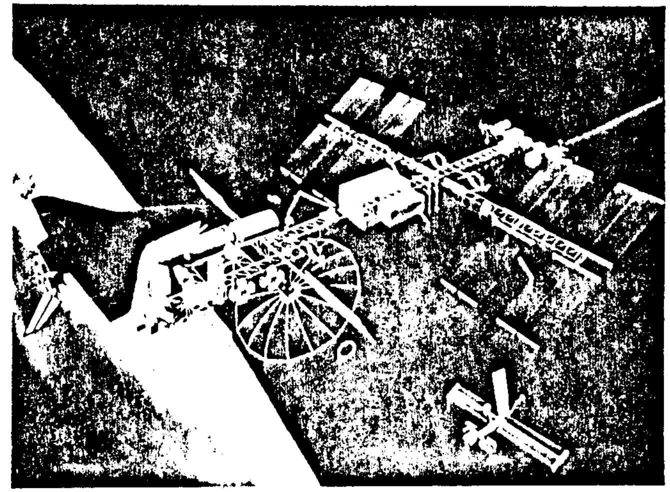


IMAGE GENERATION
IMAGE STORAGE/RETRIEVAL

LaRC

- R&T BASE
- FOCUSED TECHNOLOGY

TECHNOLOGIES FOR

- CONSOLIDATING
- AUTOMATING
- INTEGRATING

MAN/MACHINE INTERFACE

ADVANCED DISPLAY
MEDIA

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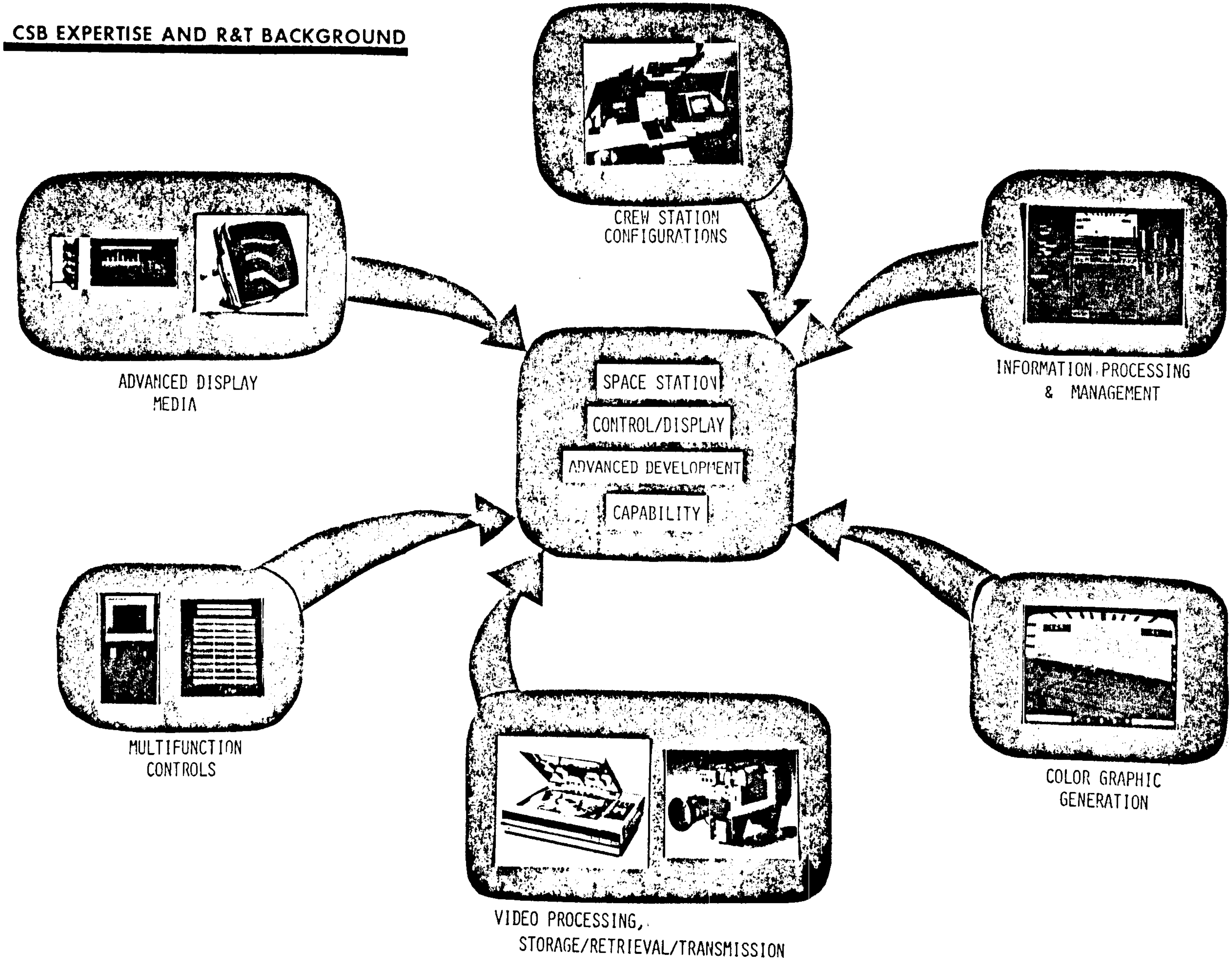
MULTI-FUNCTION
CONTROL DEVICES

INTEGRATION
METHODOLOGIES

C-4

ADVANCED INTERACTIVE CONTROL AND DISPLAY TECHNOLOGIES FOR SPACE STATION APPLICATIONS

CSB EXPERTISE AND R&T BACKGROUND



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ELECTRONIC CONTROL/DISPLAY INTERFACE TECHNOLOGY

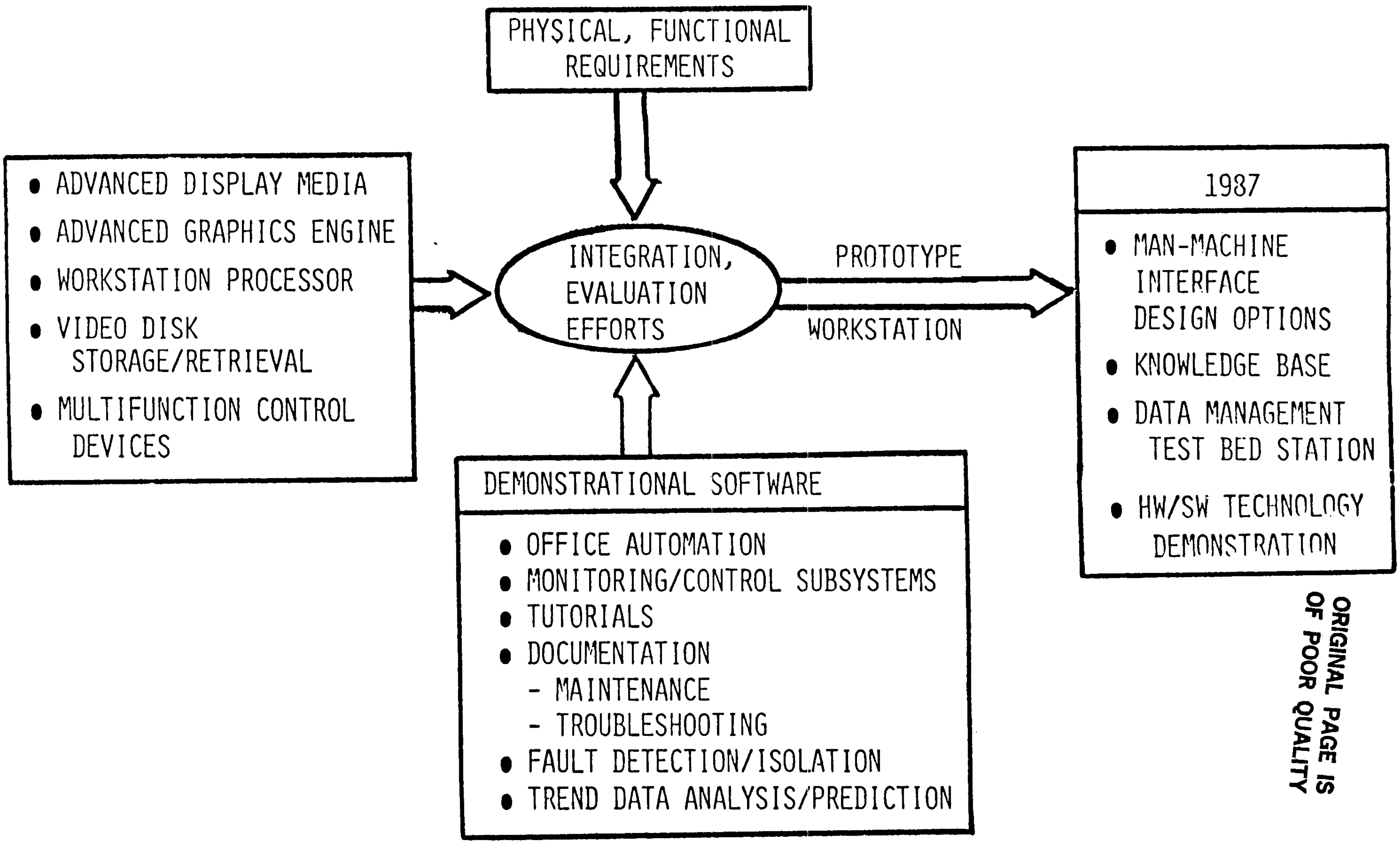
OBJECTIVE

- TO ACHIEVE THROUGH AN ORDERLY PROCESS OF ASSESSMENT ANALYSIS, DESIGN, DEVELOPMENT AND TEST, AN INTEGRATED REPRESENTATIVE WORKSTATION WHICH USES PRESENTLY AVAILABLE TECHNOLOGICAL ELEMENTS AND IS ADAPTIVE TO FUTURE EVOLUTIONARY TECHNOLOGIES, ADVANCED ARCHITECTURES, AND ENHANCED SOFTWARE.

BENEFITS

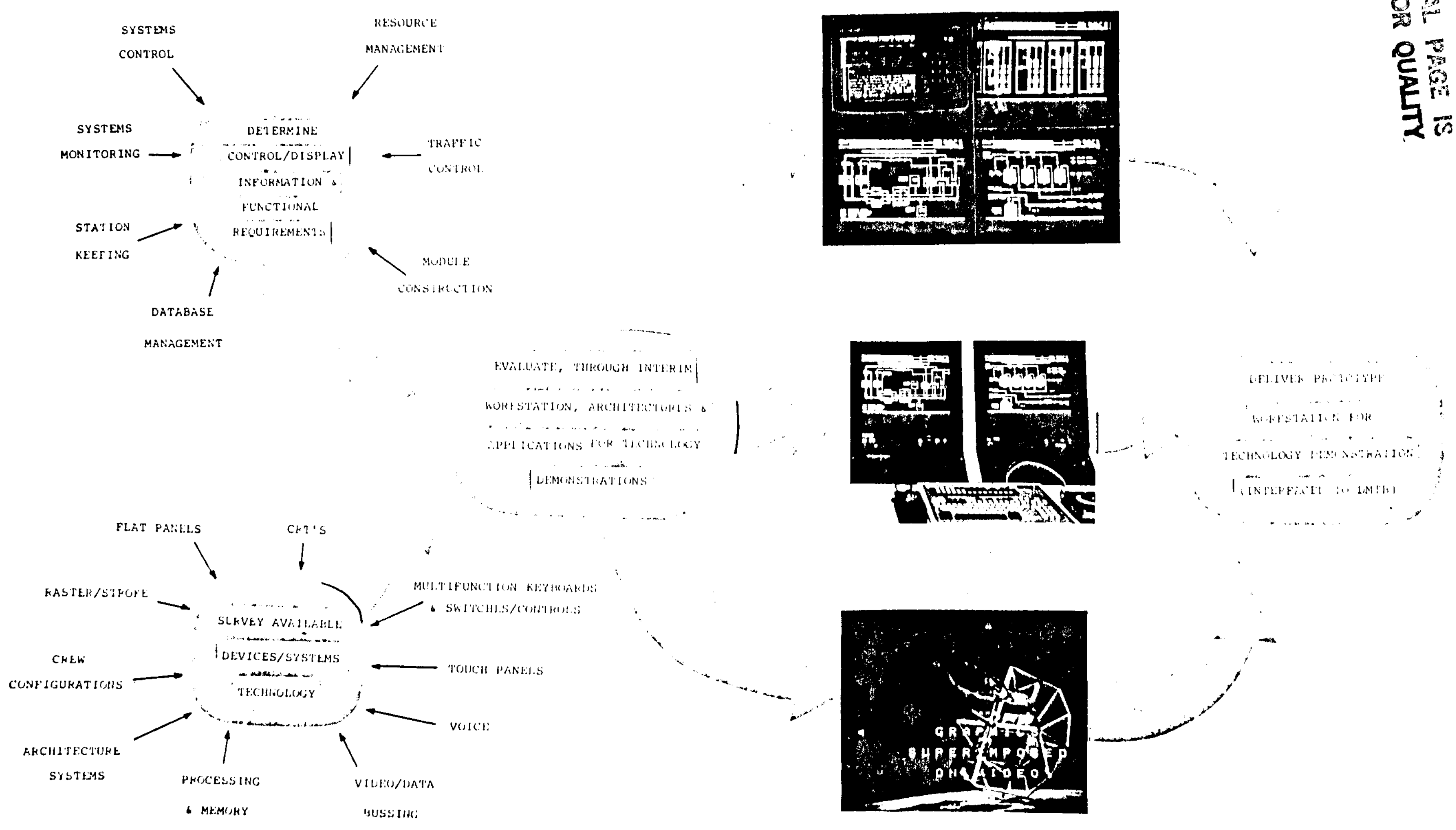
- INNOVATIVE C/D INTERFACE
- INTEGRATED DESIGN APPROACH
- REDUCED DESIGN/PRODUCTION COSTS
- IMPROVED MISSION FLEXIBILITY
- HIGHLY-RELIABLE WORKSTATIONS
- MODULARLY-EXPANDABLE SYSTEMS
- ENHANCED SAFETY/PERFORMANCE
- TRAINING MINIMIZATION

FOCUSED TECHNOLOGY: SPACE STATION ELECTRONIC CONTROL/DISPLAY INTERFACE TECHNOLOGY



ADVANCED INTERACTIVE CONTROL AND DISPLAY TECHNOLOGIES FOR SPACE STATION APPLICATIONS

PROGRAM PLAN

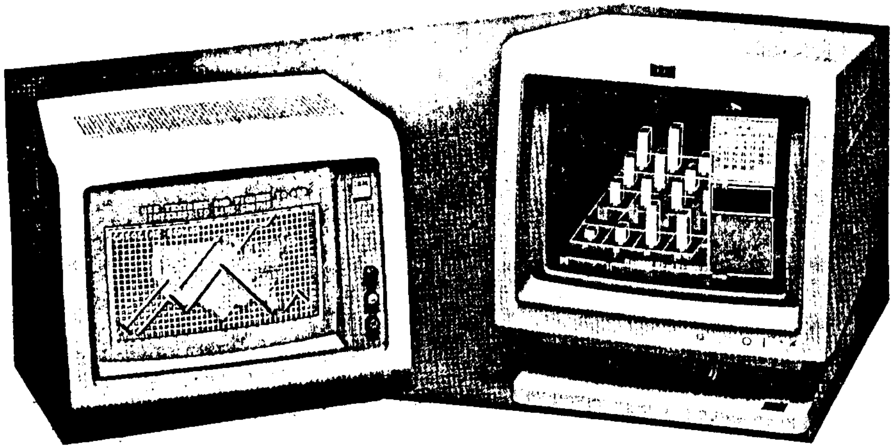


ELECTRONIC CONTROL/DISPLAY INTERFACE TECHNOLOGY

FY-85

* ANALYZE FUNCTIONAL REQUIREMENTS
* SURVEY/COMPILE CONTROL/DISPLAY TECHNOLOGY BASE INTO INTERACTIVE DATABASE (DELIVERABLE FY-87)
* ASSEMBLE INTERIM WORKSTATION
  - PROCESSOR - VIDEO DISK
  - I/O DEVICES
* SELECT APPLICATIONS FOR TECHNOLOGY DEMONSTRATIONS
  - OFFICE AUTOMATION
  - VIDEO DISK
  - VOICE I/O
  - SUB-SYSTEMS
    MONITORING/CONTROL
    TREND DATA ANALYSIS
    FAULT DETECTION

ELECTRONIC CONTROL/DISPLAY INTERFACE TECHNOLOGY
INTERIM WORKSTATION FUNCTIONAL REQUIREMENTS



DISPLAYS

* MINIMUM OF THREE FULL-COLOR, 13" OR 19", CRT's
* CONTROLLED DYNAMIC WINDOWING OF CONCURRENT DISPLAY FORMATS
* CONTROLLED VIDEO SWITCHING OF FORMATS/DISPLAYS

INPUT/OUTPUT CAPABILITIES

* PDP's
* KEYBOARD
* MINIATURE IMBEDDED TRACKBALL (WITHIN HAND-CONTROLLER)
* CONVENTIONAL TRACKBALL
* TOUCH OVERLAYS
* VOICE RECOGNITION AND SYNTHESIS

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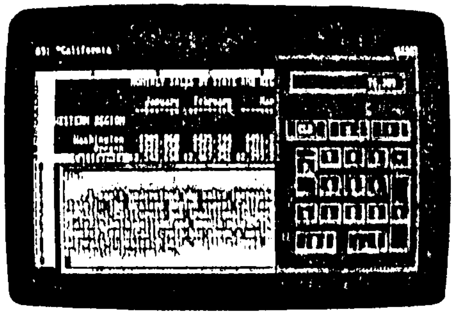
ELECTRONIC CONTROL/DISPLAY INTERFACE TECHNOLOGY

INTERIM WORKSTATION FUNCTIONAL REQUIREMENTS

VIDEO DISK UTILIZATIONS

* PREVENTIVE MAINTENANCE, UNPLANNED MAINTENANCE
* TRAINING TUTORIALS

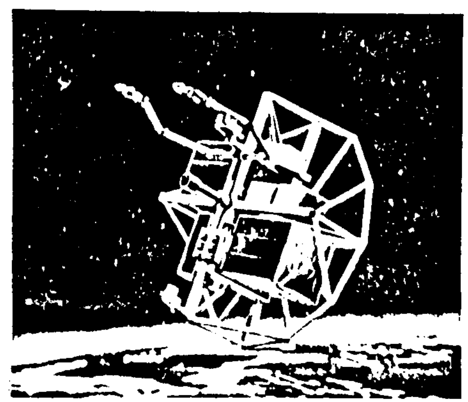


OFFICE AUTOMATION FUNCTIONS

* WORD PROCESSING
* SPREAD SHEET
* DATABASE MANAGEMENT
* SCHEDULER
* GRAPHICS PACKAGE

SUB-SYSTEM APPLICATIONS

* MONITORING/CONTROL DEMONSTRATION
* TREND DATA ANALYSIS/PREDICTION
* FAULT DETECTION/ISOLATION DEMONSTRATION
* TRAINING SIMULATIONS

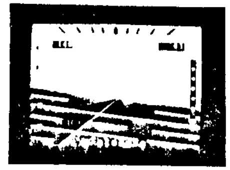
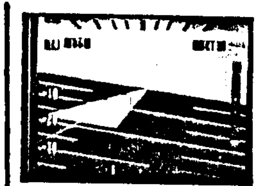
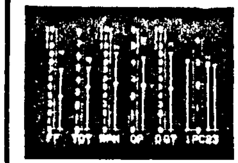


ELECTRONIC CONTROL/DISPLAY INTERFACE TECHNOLOGY

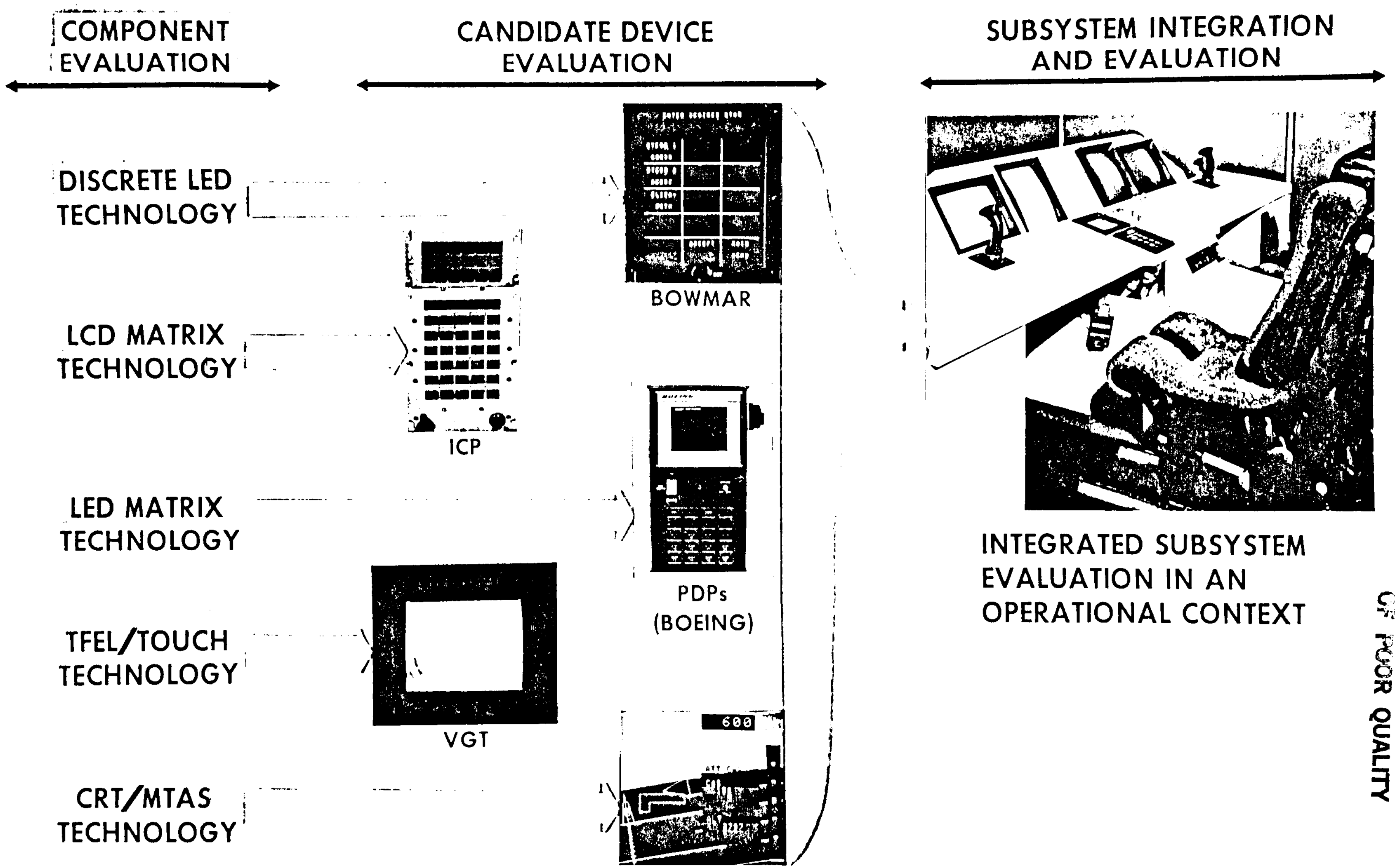
ARCHITECTURAL GOALS

- DUAL DATA BUSSES FOR FUNCTIONAL PARALLELISM AND SINGLE POINT DATA PATH FAILURE PROTECTION
- DEDICATED MULTI-PROCESSORS FOR MAXIMUM EFFICIENCY, MAINTAINABILITY AND FLEXIBILITY
- FAULT MONITORING AND AUTO-REPARTITIONING OF FAILED FUNCTIONS
- MODULAR FOR EASE OF GROWTH AND ADAPTABILITY TO DESIGN CHANGES/ IMPROVEMENTS
- NO PART REDUNDANCY
- REASONABILITY LIMIT CHECK IN S/W ON CRITICAL PARAMETERS
- INCORPORATES PRESENT TECHNOLOGIES AND IS ADAPTABLE TO EMERGING TECHNOLOGIES

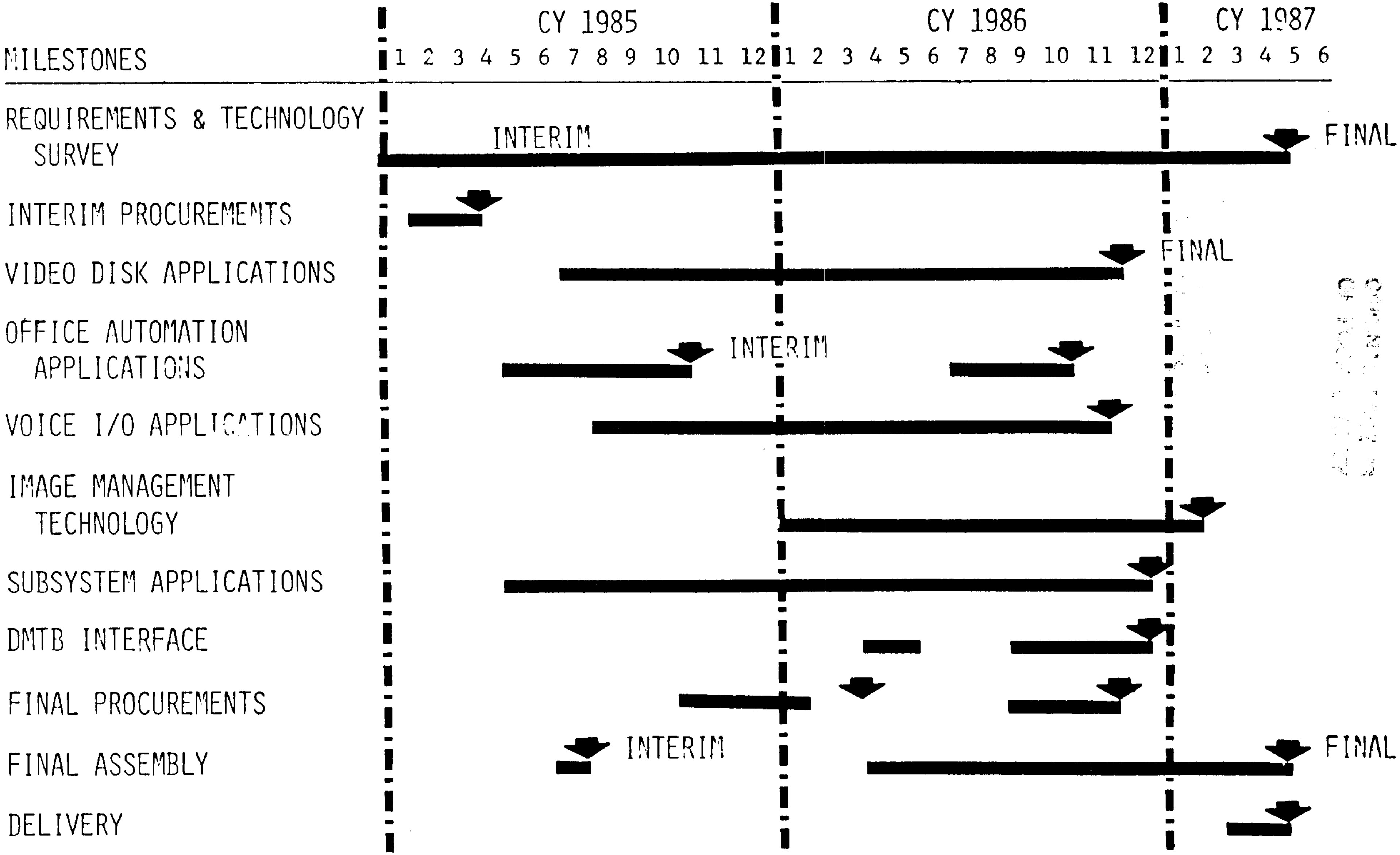
FOUR LEADING CANDIDATES FOR LARGE AREA DISPLAY

PERFORMANCE CHARACTERISTIC	COLOR CRT 	LCD 	TFEL 	LED 
HIGH RESOLUTION	✓		✓	
LOW POWER CONSUMPTION		✓	✓	
COLOR CAPABILITY	✓			PARTIAL
LOW DEPTH BEHIND PANEL		✓	✓	✓
LOW VOLTAGE OPERATION		✓	✓	✓
VIDEO RATE ADDRESSING	✓	✓	✓	✓
ENVIRONMENTAL TOLERANCE	✓		✓	✓
MEAN-TIME BETWEEN FAILURE			✓	✓
INHERENTLY RUGGED		✓	✓	✓
GRACEFUL DEGRADATION		✓	✓	✓
COST	✓			

INFORMATION MANAGEMENT TECHNOLOGIES: EMERGING I/O DEVICES



ELECTRONIC CONTROL/DISPLAY INTERFACE TECHNOLOGY SCHEDULE



VIDEO DISC TECHNOLOGY

USES

- o INTERACTIVE TRAINING
- o INFORMATION STORAGE & RETRIEVAL
  - MAINTENANCE MANUALS
  - TROUBLESHOOTING PROCEDURES & DIAGNOSTICS
  - REPAIR PARTS MANUALS
  - VIDEO/DATA/AUDIO
- o VIDEC DATA HANDLING
  - GIGA BYTES OF ON-BOARD STORAGE
  - HIGH DATA RATES
  - LOW ERROR RATES

VIDEO DISC TECHNOLOGY
(CONT.)

ADVANTAGES

- o VIDEO DISC-BASED INTERACTIVE TRAINING VS. TRADITIONAL SELF-TAUGHT COURSES
  - MORE POSITIVE STUDENT RESPONSES
  - MORE PRODUCTIVE & EFFICIENT TRAINING
  - *- TRAINING ON ACTUAL EQUIPMENT IS SAME AS TRAINING ON VIDEO DISC (.001 CONFIDENCE LEVEL)
- o INFORMATION STORAGE EXAMPLE: U.S. ARMY'S PATRIOT MISSILE SYSTEM

	CONVENTIONAL	VIDEO DISC
MANUALS	80,000 PAGES	3 DISCS 54,000 FRAMES PER DISC 1 FRAME PER 5 PAGES
WEIGHT	300 LBS.	30 LBS. (INCLUDING PLAYER & COMPUTER)

VIDEO DISC TECHNOLOGY
(CONT.)

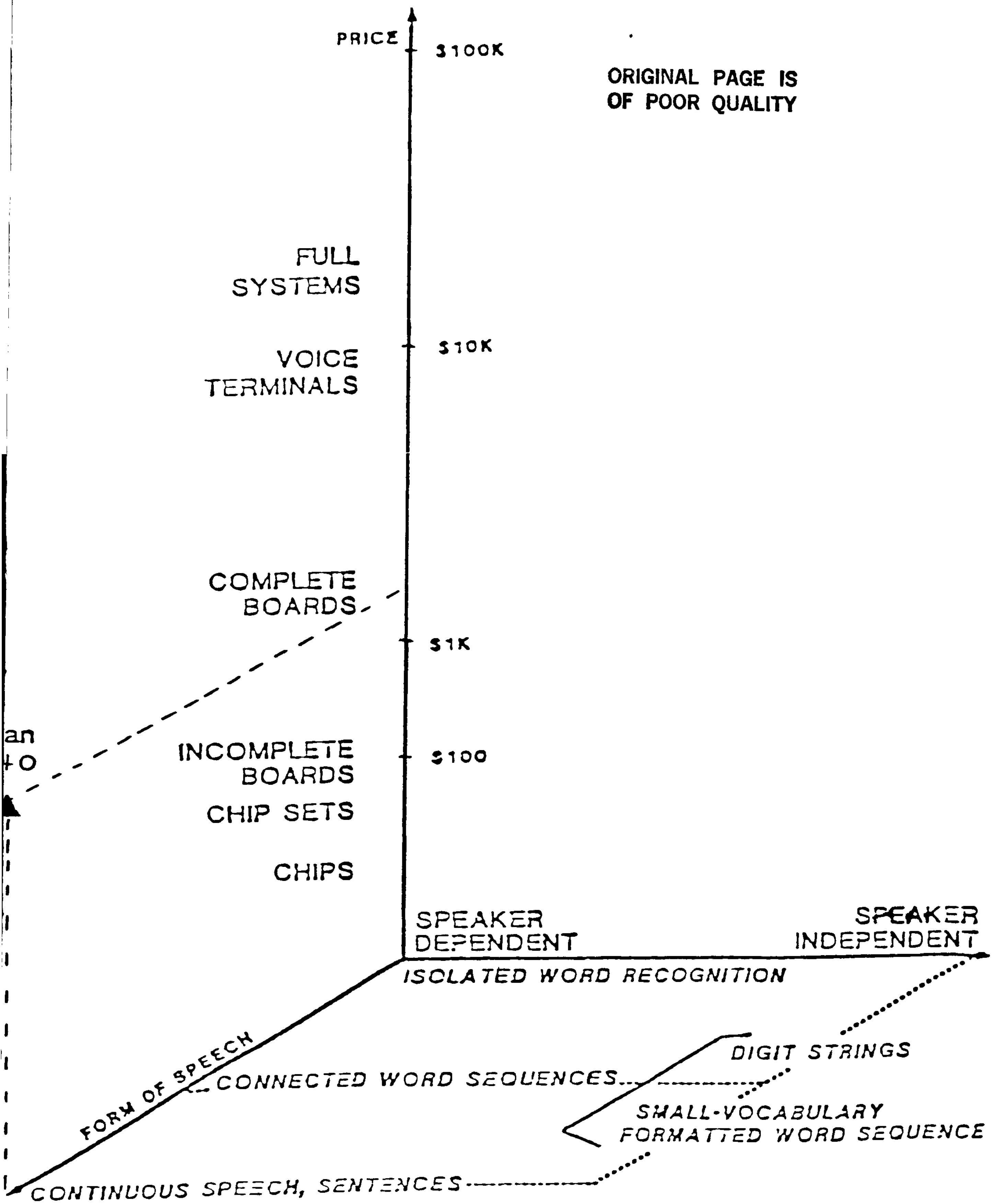
OVERALL BENEFITS

- INCREASE IN STORAGE CAPACITY/DECREASE IN SPACE & WEIGHT & COST
- COMBINED STORAGE (SINGLE MEDIA) OF VIDEO/AUDIO/DIGITAL-DATA ON ONE STORAGE MEDIUM
- INTERACTIVE CAPABILITY

POTENTIAL BENEFITS

- IMPROVED STORAGE RELIABILITY & LIFE-SPAN
- REDUCTION IN MAINTENANCE OVERHEAD
- SIMULATION OF OPERATIONAL SYSTEMS

COMMERCIAL SPEECH RECOGNIZERS



ELECTRONIC CONTROL/DISPLAY INTERFACE TECHNOLOGY

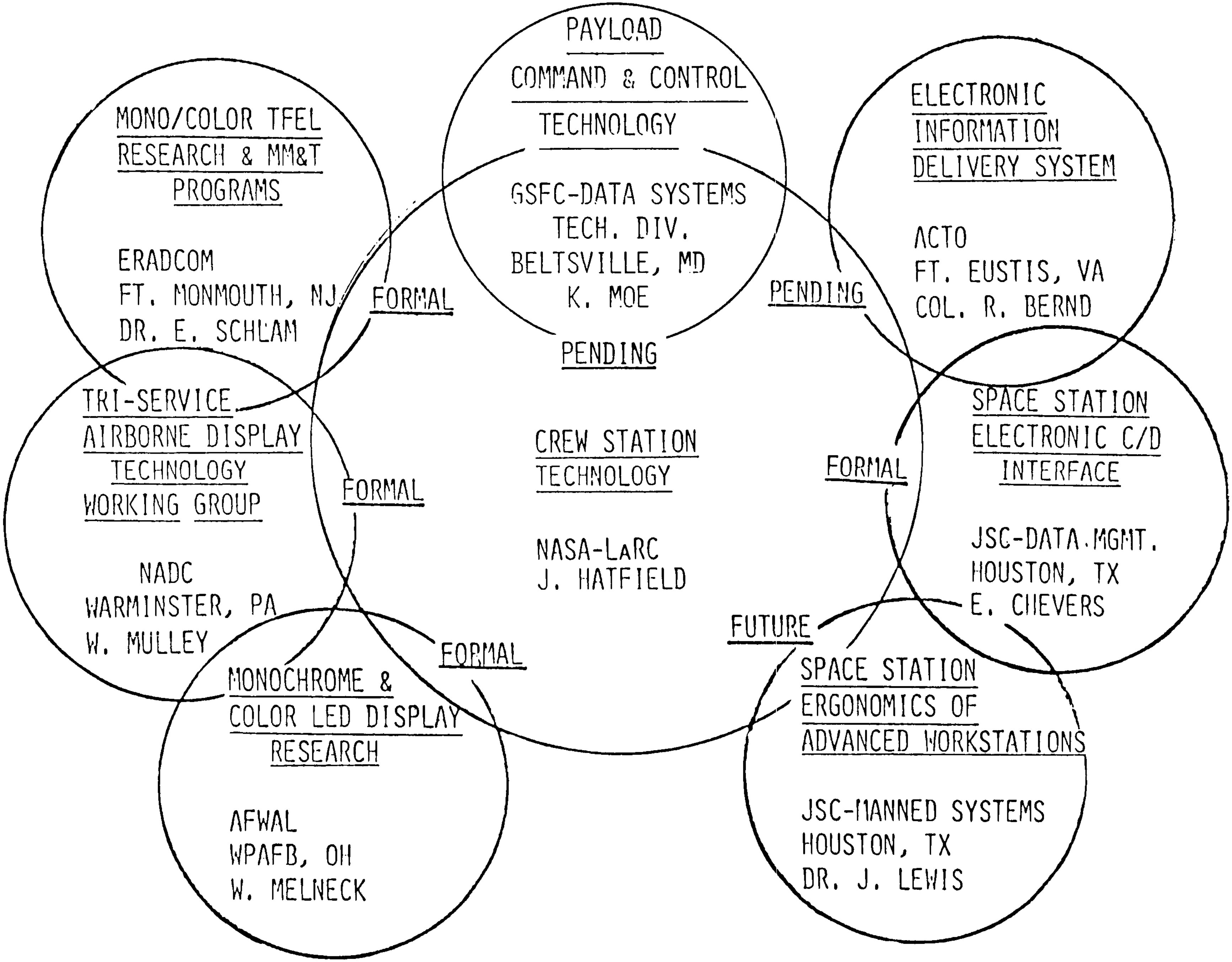
FY-86

* SURVEY/COMPILE CONTROL/DISPLAY TECHNOLOGY BASE INTO INTERACTIVE DATABASE (DELIVERABLE)
* DEVELOP APPLICATIONS
  - VIDEO DISK
    - MAINTENANCE
    - TROUBLESHOOTING
    - TUTORIAL
  - VOICE CONTROL/RMS VIEWS
* DEVELOP IMAGE MANAGEMENT SYSTEM
  - VIDEO BUS/SWITCHING
  - CONTROL TECHNIQUES
* DETERMINE JSC INTERFACE REQUIREMENTS
* SELECT/PROCURE FINAL WORKSTATION COMPONENTS (DELIVERABLE FY-87)
* INCORPORATE LARGE-SCREEN FLAT PANEL
  - MONOCHROME
  - BORROWED, FOR DEMONSTRATION ONLY

FY-87

* FINAL ASSEMBLY
  - HARDWARE
  - SOFTWARE
* DELIVERY TO JSC DATA MANAGEMENT TESTBED
* DOCUMENT WORKSTATION AND RESEARCH FINDINGS

RELATIONSHIP TO OTHER PROGRAMS



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SPACE STATION WORKSTATION TECHNOLOGY

RESOURCES SUMMARY

FUNDING	FY '81	FY '82	FY '83	FY '84	FY '85	FY '86	FY '87
R & T BASE							
CREW STATION TECHNOLOGY	$1066K	$775K	$461K	$392K	$396K	$359K	$500K
FOCUSED TECHNOLOGY							
ELECTRONIC CONTROL/ DISPLAY INTERFACE TECH.					$175K	$120K	$120K
ERGONOMICS OF ADVANCED WORKSTATIONS					-0-	$120K	$ 80K
					$175K	$240K	$200K
LARC DIRECT MAN-YEARS							
CREW STATION TECHNOLOGY	8.7 MY	13.4 MY	11.0 MY	11.4 MY	15.3 MY	15.0 MY	15.5 MY
FOCUSED TECHNOLOGY					3.0 MY	4.5 MY	4.0 MY

SUMMARY

- o EFFORT WILL PRODUCE A REPRESENTATIVE WORKSTATION FOR THE DATA MANAGEMENT TEST BED THAT PROVIDES:
  - MAN/MACHINE INTERFACE DESIGN OPTIONS FOR CONSOLIDATING, AUTOMATING, AND INTEGRATING
  - HARDWARE/SOFTWARE TECHNOLOGY DEMONSTRATIONS OF SPACE STATION APPLICATIONS
  - ADDITIONS TO THE OVERALL KNOWLEDGE BASE OF MAN/MACHINE INTERFACE DESIGN METHODOLOGIES.
- o WORKSTATION WILL EMPHASIZE:
  - ADVANCED GRAPHICS ENGINE
  - ADVANCED DISPLAY/CONTROL MEDIAS
  - IMAGE MANAGEMENT TECHNIQUES
  - MULTIFUNCTION CONTROLS
  - VIDEO DISC UTILIZATIONS

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N87-29162

P.10

USER INTERFACE AND PAYLOAD COMMAND AND CONTROL

TASK MANAGER: KAREN L. MOE
GSFC CODE 522.2
RTOP NO. 481-86-01-01 AND 481-86-02-01

TWO TASKS COMPRISE THIS OVERALL EFFORT. THE FIRST IS CONCERNED WITH DEVELOPING A MODULAR, MACHINE INDEPENDENT WORKSTATION DESIGN, SCIENCE OPERATIONS INTERFACE LANGUAGE AND INTERACTION TECHNIQUES. DESIGN CONCEPTS AND PROTOTYPE DEMONSTRATION OF A STATE OF THE ART PROTOTYPE WORKSTATION ARE TO BE BASED ON DEFINING USER REQUIREMENTS BY DETERMINING USER INTERFACE MODES, REFLECTING NEEDS IN SPACE AND ON GROUND, CENTRALIZED AND REMOTELY DISTRIBUTED. ACTUAL USER EVALUATIONS OF THIS HARDWARE/SOFTWARE WORKSTATION WILL FOLLOW THE INITIAL DEMONSTRATION. THE SECOND TASK AIMS AT GENERATING A COMMAND AND CONTROL SYSTEM DESIGN CONCEPT FOR SUPPORTING TELESCIENCE - A CONCEPT FOR INDEPENDENT SCIENCE USER OPERATIONS WITHIN AN "OPERATIONS ENVELOPE". AN EVALUATION TEST BED IS TO BE DEVELOPED IN THE '86 TIME FRAME FOR THE PURPOSE OF DEMONSTRATING THIS TELESCIENCE PAYLOAD CONTROL CONCEPT. IN PARALLEL WITH THE FOREGOING TASK, OPERATIONS CONCEPTS, SCENARIOS AND TECHNOLOGY DRIVERS FOR REMOTE USER PAYLOAD COMMAND AND CONTROL WILL BE INVESTIGATED.

USER INTERFACE AND PAYLOAD COMMAND AND CONTROL

OBJECTIVES:

- o DEFINE FUNCTIONS OF THE SPACE STATION USER INTERFACE (SPACE & GROUND, CENTRAL AND REMOTE); DEVELOP DESIGN CONCEPT, BUILD/EVALUATE PROTOTYPE USER WORKSTATION (INCLUDING USER INTERFACE LANGUAGE)

- o DEVELOP OPERATIONS CONCEPTS/SCENARIOS FOR SPACE STATION USER PAYLOAD COMMAND AND CONTROL OPTIONS; DEMONSTRATE CONCEPTS FOR IMPLEMENTING TELESCIENCE CAPABILITY

USER INTERFACE AND PAYLOAD COMMAND AND CONTROL

TECHNICAL CHALLENGES:

- o MANY USERS WITH COMMON NEEDS BUT DIFFERENT VIEWPOINTS

  FLIGHT, GROUND OPERATIONS, SCIENCE

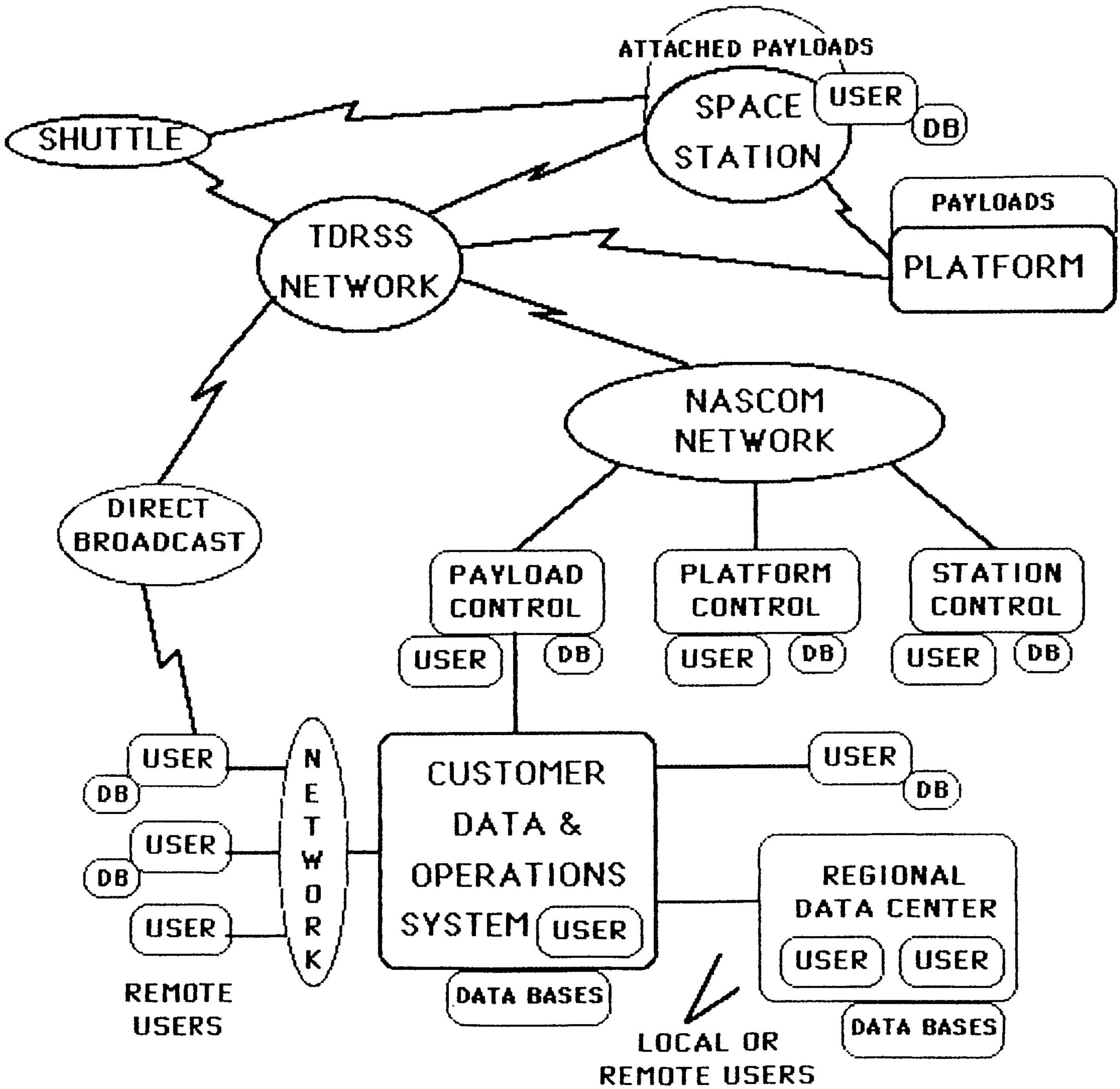
- o MANY USER FUNCTIONS AND INTERFACES TO SPACE STATION

  ACCESS TO DISTRIBUTED DATA AND SERVICE CENTERS (REGIONAL CENTERS, CDOS, POCC'S, ETC.)
  COMMUNICATIONS WITH REMOTE SYSTEMS (PAYLOAD, SPACE BASE, NETWORK, ETC.) AND OTHER USERS (INCLUDING CREW)

- o MANY DIFFERENT WAYS OF OPERATING

  ROUTINE PLAN VS DYNAMIC INTERACTION
  LEVELS OF AUTONOMY AND AUTOMATION
  IMPLICATIONS OF TELESCIENCE

POTENTIAL SPACE STATION OPERATIONAL INTERFACES



USER INTERFACE AND PAYLOAD COMMAND AND CONTROL

APPROACH AND PRODUCTS:

o USER INTERFACE LANGUAGE

TEAM-JSC, KSC, GSFC
REQUIREMENTS DEFINITION '85
USER EVALUATIONS '85-'87

o WORKSTATION

TECHNOLOGY WORKSHOP 3/85
DEVELOP WORKSTATION DESIGN CONCEPT '85
DEMO PROTOTYPE WORKSTATIONS '86
USER EVALUATIONS '86-'87

o TELESCIENCE

DEVELOP CONCEPT FOR "ENVELOPE OF OPERATIONS" '85
DEVELOP EVALUATION TESTBED '86
DEMO REMOTE PAYLOAD CONTROL '86-'87

WORKSTATION TECHNOLOGY WORKSHOP

HIGHLIGHTS:

- o 40 PARTICIPANTS
  - 10 UNIVERSITY TECHNOLOGY EXPERTS
  - 4 GOV'T LIAISONS IN WORKSTATION TECHNOLOGY
  - NASA SPACE STATION REPS (SPACE & GROUND)
  - WORKSHOP FACILITATORS

- o OVER 50 FORECASTS IN 7 AREAS GENERATED-
  - USER INTERFACE, VOICE, GRAPHICS, I/O DEVICES
  - LANGUAGES
  - DATABASE LANGUAGES AND MANAGEMENT
  - TRAINING AND SIMULATION
  - RESOURCE MANAGEMENT
  - COMMUNICATIONS
  - SOFTWARE DEVELOPMENT

- o PROMISING OR INNOVATIVE TECHNOLOGIES INCLUDED-
  - USER INTERFACE 'AUTHORING' TOOL
  - ICONIC LANGUAGES
  - DATA BASE FILTERING LANGUAGES FOR NON-SPECIFICALLY STRUCTURED DATA

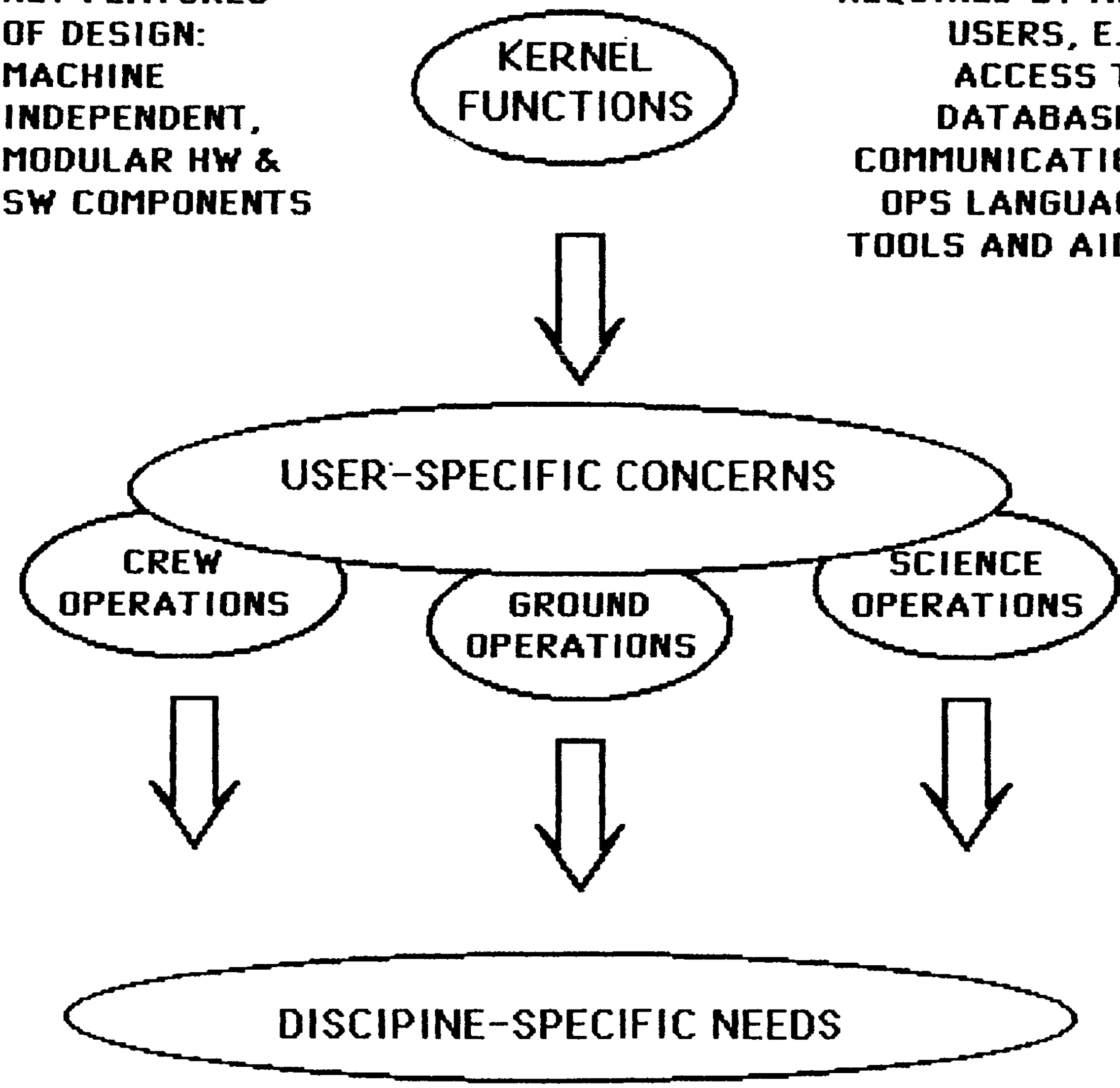
- o SIGNIFICANT TECHNOLOGY APPLICATION NEEDS INCLUDED-
  - SIMULATOR DEVELOPMENT TOOLS
  - RESOURCE SCHEDULING TECHNIQUES
  - EXPERT SYSTEM DEVELOPMENT TOOLS
  - AUTOMATED PROGRAM (CODE) GENERATION CAPABILITY

- o RESULTS OF WORKSHOP WILL GUIDE DESIGN OF WORKSTATION MODULES AND IDENTIFY TECHNOLOGY APPLICATIONS

WORKSTATION DESIGN CONCEPT

KEY FEATURES
OF DESIGN:
MACHINE
INDEPENDENT,
MODULAR HW &
SW COMPONENTS

COMMON FUNCTIONS
REQUIRED BY ALL
USERS, E.G.
ACCESS TO
DATABASES
COMMUNICATION
OPS LANGUAGE
TOOLS AND AIDS



FLIGHT CREW	SHUTTLE	ASTROPHYSICS
PAYLOAD SPEC.	SPACE STATION	COMMUNICATIONS
	SERVICING	EARTH & LIFE SCIENCE
	PLATFORM	MICROGRAVITY
	PAYLOAD	PLASMA PHYSICS
	INSTRUMENT	PLANETARY

K. MOE
3/85

TELESCIENCE DESIGN CONCEPT DEFINITIONS

TELESCIENCE CONCEPT OF OPERATIONS - SPACE STATION USER IS PROVIDED THE ABILITY TO <u>INDEPENDENTLY</u> CONTROL PAYLOAD

INDEPENDENT OPERATIONS - ABILITY TO REMOTELY OPERATE A PAYLOAD WITHOUT COORDINATING OPERATIONS THROUGH AN EXTERNAL FACILITY (E.G., POCC); IMPLIES COMPLETE KNOWLEDGE OF CURRENT OPERATIONAL RESOURCE CONSTRAINTS AND CONFIDENT RELIANCE ON THE OPERATIONAL ENVIRONMENT

OPERATIONAL ENVELOPE - DEFINITION OF LIMITS OR BOUNDS ON: <u>SHARED RESOURCES</u> WHICH THE PAYLOAD MAY DEMAND; <u>OPERATIONAL ENVIRONMENT</u> REQUIRED BY THE PAYLOAD; AND <u>OPERATIONAL ENVIRONMENT</u> WHICH THE PAYLOAD MAY IMPACT

SHARED RESOURCES - RESOURCES PROVIDED ONBOARD BY THE HOST SPACE ELEMENT (E.G., PLATFORM), INCLUDING POWER, HOST'S ATTITUDE, COMMUNICATION BANDWIDTH, DATA STORAGE, DATA PROCESSING, PHYSICAL SPACE (FIELD OF VIEW)

OPERATIONAL ENVIRONMENT - CONDITIONS IN WHICH THE HOST OR PAYLOAD OPERATES, INCLUDING CHANGES IN ANGULAR MOMENTUM, VIBRATION/JITTER, PHYSICAL POSITION, THERMAL DISSIPATION, OUTGASSING/CONTAMINATION, ELECTROMAGNETIC RADIATION

TELESCIENCE DESIGN CONCEPT KEY FEATURES

- PRE-MISSION AGREEMENT BETWEEN NASA AND USER SPECIFIES OPERATIONAL ENVELOPE, I.E., LOWER BOUNDS ON GUARANTEED NASA SERVICES AND OPERATIONAL ENVIRONMENT, AND UPPER BOUND ON USER OPERATIONAL NEEDS

- ENVELOPE CAN DYNAMICALLY EXPAND OR CONTRACT (WITHIN SPECIFIED RANGE) ALLOWING MORE EFFICIENT USE OF RESOURCES

- INDEPENDENT OPERATIONS GUARANTEED WHILE USER OPERATES PAYLOAD WITHIN OPERATIONAL ENVELOPE

- FLEXIBILITY ALLOWS RE-ALLOCATION OF RESOURCES IN REAL TIME, ALSO EASIER TO ADAPT TO NEW PAYLOAD COMPLEMENT

- MINIMIZES NASA INVOLVEMENT IN PAYLOAD OPERATIONS, USER DEFINES NOMINAL OPERATIONS INTERFACE

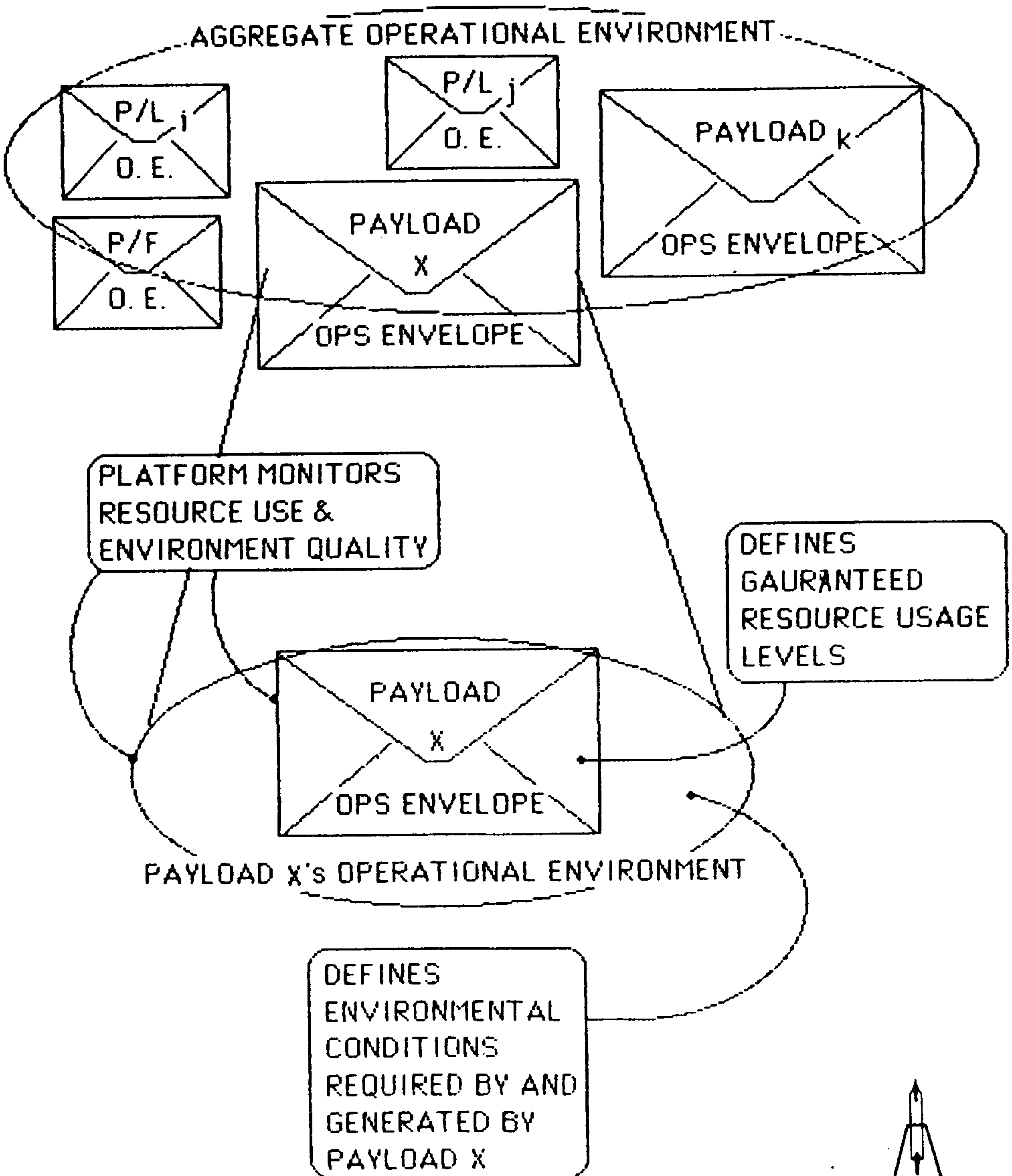
- NASA MUST PROTECT ASSETS AND AGREEMENTS WITH ALL PAYLOAD USERS AGAINST USER ATTEMPTS TO OPERATE OUTSIDE OF ENVELOPE (E.G., USER PROVIDES PAYLOAD SAFING "BUTTON")

- PRICE OR OTHER INCENTIVES WILL EXIST TO INDUCE SELF REGULATION OF PAYLOAD DEMANDS ON ONBOARD RESOURCES, OPERATIONAL ENVIRONMENT

- SYSTEM MUST BE CAPABLE OF MAINTAINING HEALTH & SAFETY OF THE HOST ELEMENT UNDER ALL CIRCUMSTANCES; WILL DRIVE ONBOARD SENSOR, COMMUNICATION, AND DATA PROCESSING TECHNOLOGY

- APPROACH MINIMIZES NEED FOR COMMAND CHECKING

TELESCIENCE OPERATIONAL ENVELOPE



N87-29163

USER DATA MANAGEMENT

P.9

RTOP MANAGER: EDWARD B. CONNELL
GSFC CODE 522
RTOP NO. 481-83-01

THE PRIMARY OBJECTIVE OF THIS EFFORT IS TO IDENTIFY, DEVELOP, AND DEMONSTRATE KEY DATA MANAGEMENT TECHNOLOGIES TO SUPPORT USER ACCESS TO SPACE STATION DATA. TO ACCOMPLISH THIS OBJECTIVE, THERE ARE SEVERAL TECHNICAL CHALLENGES WHICH MUST BE ADDRESSED. FIRST IS HOW TO PROVIDE ROUTINE CUSTOMER ACCESS TO HIGH VOLUME, DYNAMIC AND DISTRIBUTED DATA BASES. THIS ACCESS WILL ENCOMPASS THE FUNCTIONS OF MISSION AND PAYLOAD PLANNING AND OPERATIONS, DATA PROCESSING AND ANALYSIS, AND DATA ARCHIVE AND DISTRIBUTION. SECONDLY, THERE MUST BE SOME ANALYSIS OF ARCHITECTURES FOR HANDLING HIGH-VOLUME DATA STREAMS LIKE THOSE EXPECTED FROM THE SPACE STATION. THIS ANALYSIS WILL EXAMINE THE USE OF PACKETIZED VERSUS NON-PACKETIZED DATA FORMATS, MODULAR EXPANSION CAPABILITIES, REAL-TIME VERSUS NON-REAL-TIME DATA PROCESSING, AND THE INTERFACES AND ARCHITECTURE REQUIRED TO SUPPORT TELESCIENCE OPERATIONS. THE TASK WILL ALSO DETERMINE BENCHMARKS OF PERFORMANCE CAPABILITIES FOR TECHNOLOGY OPERATIONS, SUCH AS VARIED DATA BASE STRUCTURES, DATA ACCESS PROCEDURES, DISTRIBUTED DATA BASE DESIGN, AND DATA BASE MACHINES, IN AN END-TO-END ENVIRONMENT.

USER DATA MANAGEMENT

E. CONNELL

OBJECTIVE:

PROTOTYPE AND EVALUATE DATA MANAGEMENT SYSTEM ELEMENT AND ARCHITECTURE OPTIONS FOR USER PAYLOAD AND SUPPORTING DATA

TECHNICAL CHALLENGES:

- PROVIDE EASY-TO-USE, ROUTINE CUSTOMER ACCESS TO HIGH VOLUME, DYNAMIC, GEOGRAPHICALLY DISTRIBUTED DATA BASES

FUNCTIONS

- MISSION AND PAYLOAD PLANNING & OPS
- DATA PROCESSING AND ANALYSIS
- DATA ARCHIVE AND DISTRIBUTION

DATA & ASSOCIATED CATALOGS

- GROUND AND ONBOARD DATA BASES
- SCIENCE, ENGINEERING, ANCILLARY DATA
- CORRELATIVE AND REFERENCE DATA
- SCHEDULES, MISSION HISTORIES

- ANALYZE ARCHITECTURES FOR HANDLING HIGH-VOLUME DATA STREAMS
  - 100 MBPS AVERAGE THROUGHPUT, 300-600 MBPS PEAK
- DETERMINE REAL BENCHMARKS OF PERFORMANCE CAPABILITIES

APPROACH

- TEST AND EVALUATE SELECTED DATA MANAGEMENT TECHNOLOGY OPTIONS IN AN END-TO-END ENVIRONMENT
  - DATA BASE STRUCTURES
  - DATA ACCESS PROCEDURES
  - DISTRIBUTED DATA BASE DESIGNS
  - DATA BASE MACHINES
- EVALUATE DISTRIBUTED DATA MANAGEMENT ARCHITECTURE OPTIONS
- EXTEND COMPLETED STUDIES OF HIGH-RATE DATA HANDLING COMPUTERS TO:
  - BENCHMARK PERFORMANCE, IN REAL-WORLD ENVIRONMENT, FOR PACKETIZED AND NON-PACKETIZED FORMATS
  - EXPLORE MODULAR EXPANSION CAPABILITIES (3 → 30 → 300 MBPS THROUGHPUT)
  - ASSESS INTERFACES AND ARCHITECTURE REQUIRED TO SUPPORT TELESCIENCE OPERATIONS
  - ANALYZE TECHNOLOGY DRIVERS AND OPTIONS

DELIVERABLES

- CONCEPTUAL DESIGN, BENCHMARKS FOR SELECTED DATA MANAGEMENT TECHNOLOGY AND SYSTEM OPTIONS
- ASSESSMENT AND RECOMMENDATIONS FOR APPROACH TO USER DATA MANAGEMENT
- DEFINITION AND EVALUATION OF DATA HANDLING CENTER ARCHITECTURE OPTIONS, INCLUDING BENCHMARK TESTING
- TECHNOLOGY DRIVER OPTIONS ASSESSMENT

STATUS

DATA MANAGEMENT

- NOT FEASIBLE TO REPLICATE DATA BASES IN ONE CENTRAL LOCATION
  - TOO MANY
  - TOO LARGE
  - DYNAMIC
  - LIMITED DOWNLINK BANDWIDTH
- NOT REALISTIC TO REQUIRE THAT ALL DATABASES BE STRUCTURED IDENTICALLY
  - WIDELY VARYING REQUIREMENTS
- SCOPE OF SPACE STATION DATA MANAGEMENT PROBLEM MORE LIMITED THAN GENERAL CASE
  - USERS HAVE A GENERAL IDEA OF WHAT THEY NEED
    - IMPLIES LIMITED "BROWSE" REQUIREMENT
  - USERS TYPICALLY REQUEST DATA, BUT DO NOT UPDATE DATABASES
    - LIMITED REMOTE DATABASE MANIPULATION REQUIREMENT
- POTENTIAL SOLUTIONS IN CODE R, T BASE PROGRAMS
  - DATABASE UNIFORMIZATION
  - STANDARD FORMAT DATA UNITS (DATA "SHELL")

STATUS

- AREAS OF UNCERTAINTY
  - "DEPTH" AND UPDATE FREQUENCY OF CENTRAL CATALOG
  - UPLINK TRAFFIC
  - HANDLING OF MULTIPLE USER REQUESTS
    - VIRTUAL CIRCUIT
    - PACKETS
  - PERFORMANCE
    - HARDWARE/SOFTWARE SPEED
    - PHYSICAL LIMITS (E.G., DELAYS DUE TO MULTIPLE SATELLITE HOPS)

STATUS

HIGH-RATE DATA HANDLING

- SPACE STATION PAYLOAD DATA HANDLING REQUIREMENTS ARE A MAJOR CHALLENGE
  - MODULAR GROWTH TO 100 MBPS THROUGHPUT, PEAK RATES 300-600 MBPS
  - DATA THROUGH SYSTEM IN LESS THAN 2 ORBITS (BUT OFTEN MUST BE HELD FOR MORE THAN ONE ORBIT)
  - UP TO 20% OF DATA PROCESSED IN REAL TIME FOR POCC'S, SOC'S
- TELESCIENCE OPERATIONS REQUIRE REAL-TIME RECONFIGURATION CAPABILITY TO ACCOMMODATE DIFFERENT INSTRUMENT OPERATING MODES
- "GUARANTEED" DATA DELIVERY MAY REQUIRE SUBSTANTIAL MASS STORE CAPABILITY
  - TRADE: SHORT DATA "HOLD TIME" ⇒ MINIMUM STORAGE COST AT DATA HANDLING CENTER
HIGH-SPEED DATA VALIDATION CAPABILITY AT USER FACILITIES
USER FACILITIES OPEN AROUND THE CLOCK

    LONG DATA "HOLD TIME" ⇒ HIGH COST MASS STORE AT DATA HANDLING CENTER
LOWER COST DATA VALIDATION AT USER FACILITIES
EIGHT HOURS/DAY, FIVE DAYS/WEEK STAFFING AT USER FACILITIES

    EXAMPLE: AT 100 MBPS, A 24 HOUR "HOLD" REQUIRES 8.6×10^{12} BITS STORAGE
A 30 HOUR "HOLD" REQUIRES 2.6×10^{14} BITS STORAGE

STATUS

- BENCHMARKS ON CDC ADVANCED FLEXIBLE PROCESSOR SHOW CLEAR PERFORMANCE ADVANTAGE FOR PACKETIZED DATA
  - 4:1 IMPROVEMENT IN THROUGHPUT WITH PACKETS OVER TDM
- KEY ANALYSIS AREA: PERFORMANCE IMPROVEMENTS OBTAINABLE THROUGH ONBOARD PROCESSING, DATA HANDLING
  - CALIBRATION
  - ANCILLARY DATA MERGING
  - "FORWARD-ONLY" DATA (NO REVERSED TAPE RECORDER DATA)

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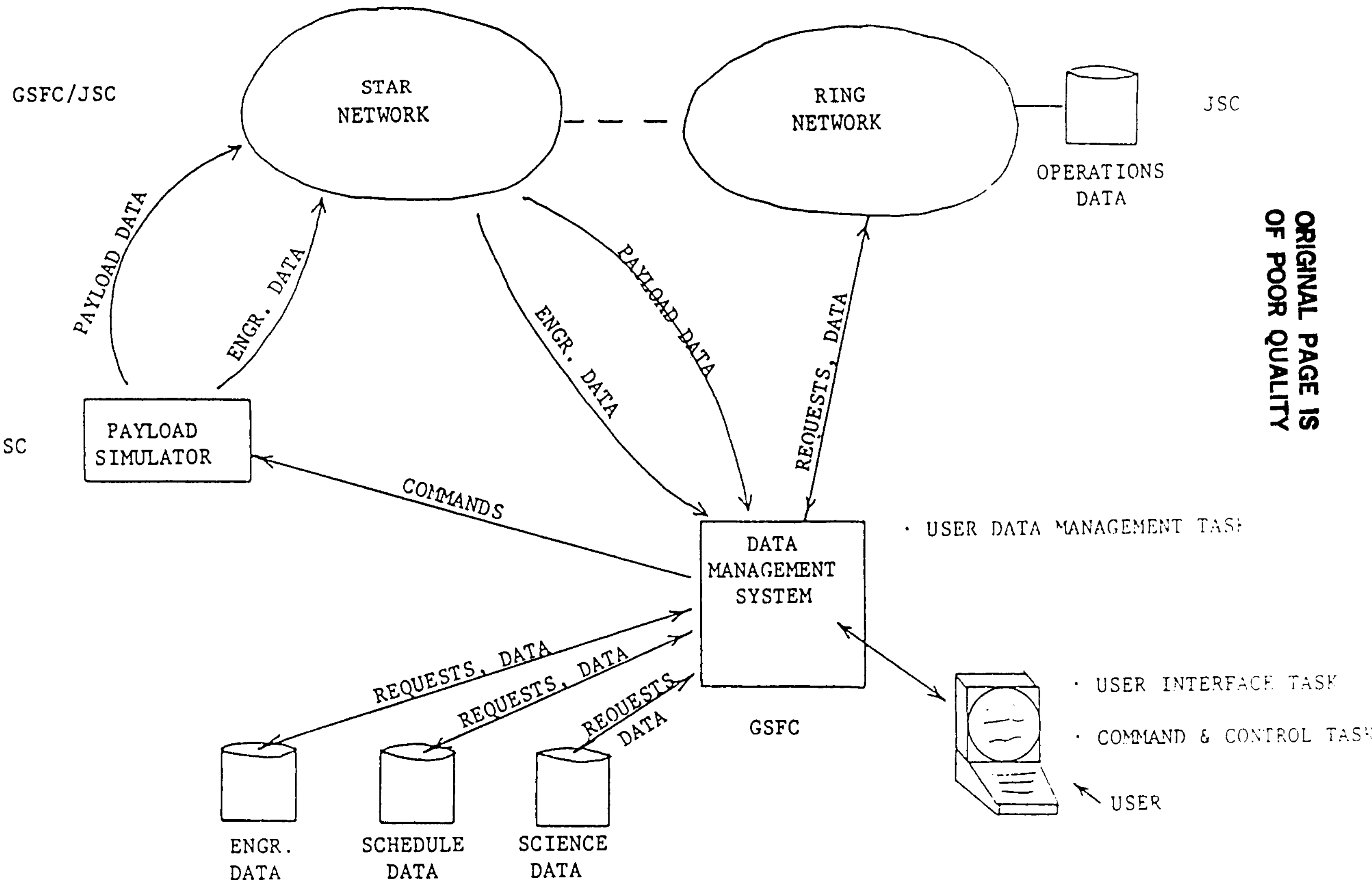

TESTBED EXPERIMENT

CENTER	MILESTONE SCHEDULE	LEVEL	ORIG. SCHED. APPR. ____ (DATE)
RESPONSIBILITY: APPROVAL ____	PROJECT Code 500 Advanced Development		LAST SCHED. CHG. ____ (DATE)(NO.)(INITIALS)
ACCOMPLISHMENT ____			STATUS AS OF ____ (DATE) (INITIALS)

	MILESTONES	19 85												19 86												19 87											
		J	F	M	A	M	J	J	A	S	O	N	D	J	F	M	A	M	J	J	A	S	O	N	D	J	F	M	A	M	J	J	A	S	O	N	D
1	Data Handling System Benchmarks										▽																										
2	and Technology Drivers						▽				▽																										
3	Ada Evaluation																	▽																			
4	Distributed S/W Tools																											▽									
5	User I/F Requirements												▽																								
6	Workstation Prototype																											▽									
7	Payload OPS Concept												▽																								
8	C & C Design Recommendation																											▽									
9	Data Management Options																		▽																		
10	Conceptual Design, Benchmarks																											▽									
11																																					
12	Space Station Level B Milestones																																				
13	Reference Update Review 2									▽																											
14	Interim Requirements Review												▽																								
15	System Requirements Review															▽																					
16	Interim Systems Review																		▽																		
17	System Design Review																							▽													
18	Phase C/D ATP																																				
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NOTES:

GSFC

NASA Form 1304a (MAY 1966)

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Advanced Software Tools

Space Station Focused Technology

April 18, 1985

Robert W. Nelson

Goddard Space Flight Center

Advanced Software Tools

Drivers

Space Station data management system:

- highly distributed
- payload users controlling experiments and processing payload data from home facilities

Software:

- closely coupled modules separated by great distances (e.g. ground and space systems)
- requires specialized testing and validation
- need to characterize maintenance & evolution

482-58-16-02
18 April 1985

Advanced Software Tools

RTOP Thrusts

- Evaluate available Ada software development environments and tools
- Enhance the capability of currently available software development tool environments to meet requirements for Space Station
- Design advanced software tools for testing of distributed systems

482-58-16-02
18 April 1985

Progress To Date

Environments Acquired:

- -DEC VAX Ada (Beta Site Version)
- -Ada Language System (SofTech)
- -Data General Ada Development Environment
- -Telesoft_Ada

Evaluations Initiated:

- -Ada environments
- -Ada pilot projects
- -alternative implementation languages

Coordination:

- -Ada User's Group (formed at GSFC)
- -JSC Ada Beta Test Site
- -Space Station Software Working Group

482-58-16-02
18 April 1985

Environment Evaluation - Tools

	Compiler	Editor	Linker	Exporter	Debugger	File Manager	Command Language	User-supplied Tool-Interface	Formatter	Analyzers
SofTech ALS	x	x	x	x	x	x	x	x	x	x
DEC VAX Ada	x	x	x		x		x			
Telesoft_Ada	x	x	x							
DG ADE	x	x	x		x				x	
Verdix Ada	x	x	x		x					

482-58-16-02
18 April 1985

Environment Evaluation - General

Environment		Comments
SofTech Ada Language System	-	Severe performance limitations
	+	Rehostable; retarget capability
	-	Needs more robustness in tools
VAX Ada	+	Integrated with VMS 4.1
	+	Good performance (depending on user loading)
	-	No retargeting capability
Telesoft_Ada	-	Incomplete versions used for year
	-	Not yet validated for VAX
	-	Marginal performance
Data General Ada Dev. Environment	+	Complete environment for DG computers
Verdix Ada	+	Rapid compilation
	+	Good error diagnostics
	+	Production-quality code
	+	Split-screen debugging
	-	Uses UNIX BSD 4.2

482-58-16-02
18 April 1985

Environment Evaluation Criteria

Consistency - predictability,
portabilty of Ada user code

Efficiency

User friendliness

Portability of knowledge of tools

Supports division of labor in software development

Configuration management capabilities

482-58-16-02
18 April 1985

-Elisabeth Brinker

Pilot Ada Projects

	Size (LOC)	Environment Utilized	Comments
Attitude Dynamic Simulator for Gamma Ray Observatory	40,000	VAX Ada	Parallel development in FORTRAN
Network Control Program	5,000	VAX Ada	VAX, 8086 Target
Demultiplexer for POCC	1,000	ALS	

482-58-16-02
18 April 1985

Use of Ada Evaluation Criteria

Time to obtain a working knowledge of Ada syntax and methodology

Training methods to be used

Methodology to be applied

Time required for program design, coding, debugging

Modularity

Program size

Features of the language actually utilized

-Robert Murphy

482-58-16-02
18 April 1985

Extending the Environments

- o Examine issues related to inclusion of user-supplied tools in APSE's

- o Develop requirements and preliminary design of a tool for testing and validation for distributed system developments

  - current debuggers are for uni-processor applications

  - capture and replay intertask communication in multi-tasked, distributed processor systems

482-58-16-02
18 April 1985

FY85 Plans

Complete evaluation of Ada Environments

Complete language evaluation task

Specify tools required for debugging distributed software

Continue coordination with
- -Software Working Group
- -Software Development Environment
- -JSC Ada Beta Test Site

482-58-16-02
18 April 1985

N87-29165

SS FOCUSED TECHNOLOGY: GATEWAYS AND NOS'S

R. HARTENSTEIN
NASA GODDARD SPACE FLIGHT CENTER
APRIL 18, 1985

ABSTRACT

THIS PAPER DISCUSSES THE EXTENSIONS AND ENHANCEMENTS OF THE FIBER OPTIC DATA BUS TECHNOLOGY SUPPORTED BY THE SPACE STATION FOCUSED TECHNOLOGY PROGRAM. THIS INCLUDES THE OPERATING SOFTWARE FOR THE NETWORK CALLED THE NOS (NETWORK OPERATING SYSTEM); GATEWAYS AND GRIDGES FOR MULTIPLE NETWORK TOPOLOGIES; AND VLSI IMPLEMENTATIONS TO SHRINK THE SIZE (AND POWER) OF THE BIU DOWN TO MORE MANAGEABLE DIMENSIONS.

THE NOS APPROACH IS TO EVALUATE EXISTING SYSTEMS AND BUILD UPON THE BEST FOUNDATION AVAILABLE. THE GATEWAY/BRIDGE EFFORT IS TO DEVELOP THE SIMPLEST ELEMENTS BASED AS MUCH AS POSSIBLE ON THE EXISTING BIU'S (BUS INTERFACE UNIT) TECHNOLOGY AND DESIGNS. THE GATEWAY MUST BE MODULAR TO ACCEPT THE "FRONT END" OR PHYSICAL PECULIARITIES OF UNKNOWN DATA BUS MEDIA AS WELL AS MUCH OF LAYER 2 (THE ACCESS PROTOCOLS). IT IS THEREFORE NOT REALLY A SINGLE ELEMENT BUT A SYSTEM OF MODULES THAT CAN BE ADDED TO THE FRAMEWORK MODULE TO CUSTOM TAILOR THE GATEWAY FOR THE TWO PECULIAR NETWORKS INVOLVED. THE VLSI WORK IS INVESTIGATING TWO TECHNOLOGIES: C-MOS FOR THE LOWER SPEED (PARALLEL) LOGIC AND GALLIUM ARSENIDE, GAAS, FOR THE HIGH SPEED (SERIAL) LOGIC.

GSFC

FIBER OPTIC DATA BUS

TECHNOLOGY

	OAST	SSFT
• STAR BUS TECHNOLOGY	X	
• COMPONENT QUALIFICATION	X	
• NOS/DOS PROTOTYPE		X
• GATEWAY / BRIDGE		X
• VLSI IMPLEMENTATION		X
• FUTURE DIRECTIONS		X

SPACE STATION DATA SYSTEM

PROBLEMS :

1. HIGH BANDWIDTH SENSORS
2. LARGE NUMBER OF USERS
3. CONSTANT TURNOVER OF USERS
4. INDEPENDENCE OF USER OPS
5. TRANSPARENCY TO USER
6. AUTOMATION/ROBOTICS PROCESSING
7. AI (EXPERT SYSTEMS) DATA BASES
8. INDEFINITE LIFE TIME
9. EASE OF INTEGRATION / DEINTEGRATION
10. ISOLATION (SAFETY) OF CORE SYSTEM

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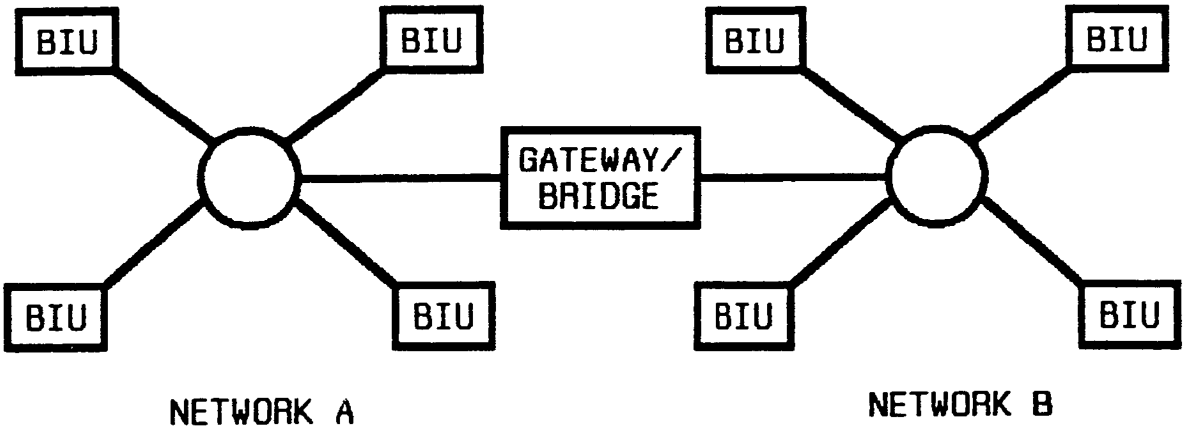

GATEWAY / BRIDGE

TYPICAL CONNECTIONS

NETWORK GATEWAY

- NETWORK GATEWAY PROVIDES THE MEANS TO EXPAND SERVICE TO MORE THAN 32 USERS

- A CLUSTER OF PASSIVE STAR NETWORKS CAN BE CONNECTED VIA NETWORK GATEWAYS

- THE DESIGN WILL INCLUDE MESSAGE ROUTING, BUFFERING, INTERNETWORKING PROTOCOLS, ETC.

- BRASSBOARD BIU WILL FORM BASIS OF THE NETWORK GATEWAY DESIG

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VLSI IMPLEMENTATION

- LOW SPEED [CMOS]
  - PARALLEL LOGIC
  - IN HOUSE CUSTOM LSI DESIGN
  - CMOS FOUNDRY SUPPLIED

- HIGH SPEED [GaAs]
  - SPERRY CONVERSION OF ECL
  - ON-GOING EFFORTS :

    LEWIS CONTRACT WITH HONEYWELL
    (STANDARD CELL)

    GSFC CONTRACT WITH ROCKWELL
    (ARMY, DARPA, OAST, 8 BIT SLICE)

    DARPA CONTRACT WITH MDAC
    (2901 BIT SLICE)

GSFC

NETWORK OPERATING SYSTEM

SHORT TERM OBJECTIVE

IS TO DEVELOP A PROTOTYPE NETWORK OPERATING SYSTEM

FOR A 100 MEGABIT / SECOND FIBER OPTIC DATA BUS.

IMPORTANT TO SPACE STATION BECAUSE

CUSTOMER INTERFACE SOFTWARE NEEDS TO BE DEVELOPED TO SUPPORT A LARGE NUMBER OF INDEPENDENTLY OPERATED INSTRUMENTS AND PAYLOADS

GSFC

LONG TERM OBJECTIVE

IS TO ESTABLISH GUIDELINES FOR WRITING A DETAILED SPECIFICATION FOR A SPACE STATION NETWORK OPERATING SYSTEM.

TO BE STUDIED :

- IMPLEMENTATION OF ISO / OSI STANDARD
- BUS ARBITRATION EFFICIENCY
- REMOTE DIAGNOSTICS
- RELIABILITY
- NOISE SENSITIVITY
- ERROR DETECTION AND HANDLING

G S F C APPROACH TO DEVELOPING AN NOS :

- AN NOS STATE-OF THE-ART STUDY
- AN RFP FOR A PROTOTYPE NOS

COMMERCIALLY AVAILABLE SYSTEMS

UNIX BASED

UNIVERSE_NET	BY	CHARLES RIVER DATA SYSTEMS
NFS	BY	SUN MICROSYSTEMS

IBM—PC BASED

NET/ONE	BY	UNGERMANN—BASS
NETWARE	BY	NOVELL, INC.

MAJOR MILESTONES

* STATE OF THE ART STUDY REPORT	5/85
* AWARD OF PROTOTYPE NOS (COMPETED) CONTRACT	7/85
* SOFTWARE REQUIREMENTS REVIEW	9/85
* PRELIMINARY DESIGN REVIEW	1/86
* CRITICAL DESIGN REVIEW	7/86
* DELIVERY OF PROTOTYPE NOS	12/86

GSFC

N87-29167

P.10

NETWORK OPERATING SYSTEM FOCUS TECHNOLOGY

RTOP 482-58-19-02

AN ACTIVITY STRUCTURED TO PROVIDE SPECIFIC DESIGN REQUIREMENTS AND SPECIFICATIONS FOR THE SS DMS NETWORK OPERATING SYSTEM (NOS) BY THE 1987 PHASE C/D RFP IS OUTLINED. EXAMPLES ARE GIVEN OF THE TYPES OF SUPPORTING STUDIES AND IMPLEMENTATION TASKS PRESENTLY UNDERWAY TO REALIZE A DMS TEST BED CAPABILITY TO DEVELOP HANDS-ON UNDERSTANDING OF NOS REQUIREMENTS AS DRIVEN BY VARIOUS ACTUAL SUBSYSTEM TEST BEDS PARTICIPATING IN THE OVERALL JSC DMS TEST BED PROGRAM. DISCUSSION IS PROVIDED OF A BASIC NOS CONCEPT BASED ON A RECENTLY COMPLETED FY-85 STUDY WHICH PRESENTS A SET OF MINIMUM AND MAXIMUM NOS REQUIREMENTS CONSISTENT WITH A MODULAR/DISTRIBUTED DMS CONCEPT.

NASA OAST
COMPUTER/SCIENCE/DATA SYSTEMS
TECHNICAL SYMPOSIUM

FOCUS TECHNOLOGY 482-58-1902
NETWORK OPERATING SYSTEM

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NETWORK OPERATING SYSTEM	AVIONICS SYSTEMS DIVISION	
	P. E. SOLLOCK	APRIL 1985

OBJECTIVE: DEVELOP, PROOF TEST AND DELIVER A SET OF DETAILED DESIGN REQUIREMENTS FOR SS DMS NOS TO SUPPORT PHASE C/D RFP

RATIONALE: DMS IS INTEGRATING MEDIA FOR ALL SS DISTRIBUTED SYSTEMS AND SYSTEM/DMS INTERFACE MUST BE STABLE AND WELL DEFINED TO ALLOW RESPECTIVE VENDOR(S) DEVELOPMENT OF EACH SYSTEM.

APPROACH: USE SS DMS TEST BED HANDS-ON INTEGRATION OF REPRESENTATIVE SYSTEM(S) TEST BEDS (D&C, PM&D, ECLSS, C&T,...) TO FORMULATE VALID SET OF DMS SERVICES AND NOS REQUIREMENTS.

NOS FY-85 MAJOR ACTIVITIES	AVIONICS SYSTEMS DIVISION	
	P. SOLLOCK	APRIL 1985

o NETWORK TECHNOLOGY COMMUNICATIONS ASSESSMENT (LEMSCO SUPPORT CONTRACT)

o NOS FUNCTIONAL REQUIREMENTS STUDY (LEMSCO/UNIVERSITY CONSULTANT)

o LAYER 7 REQUIREMENTS DEFINITION STUDY (AT&T; CANCELED AFTER FIRST REPORT)

o ADA SUITABILITY FOR NOS DESIGN/DEVELOPMENT STUDY (CSDL)

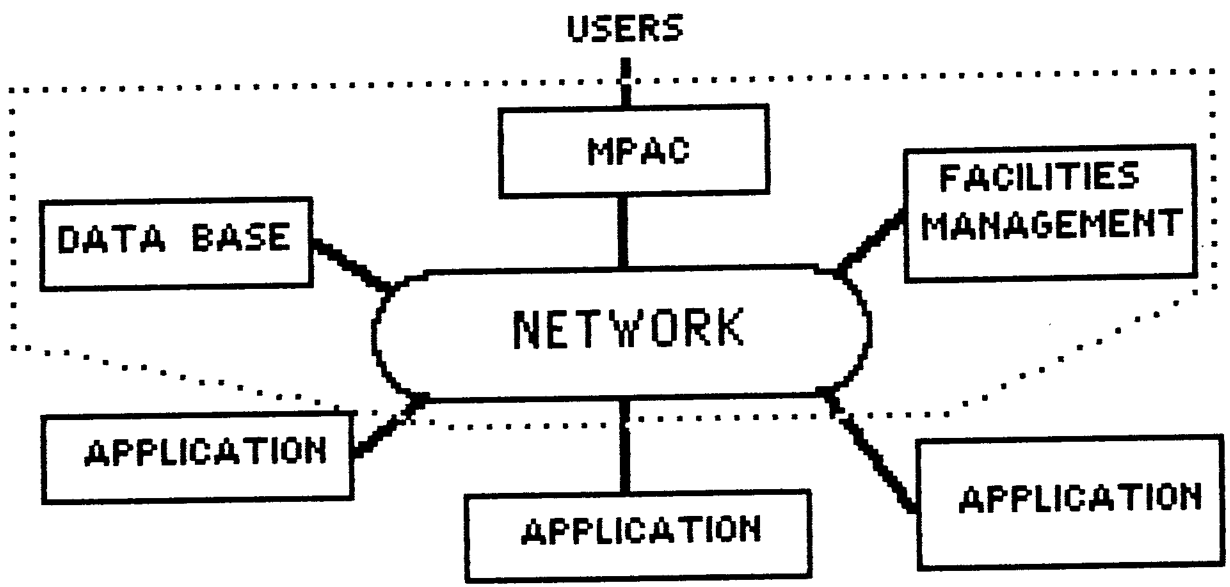
o DEFINITION/DEVELOPMENT OF DMS USERS GUIDE (LEMSCO SUPPORT CONTRACTOR)

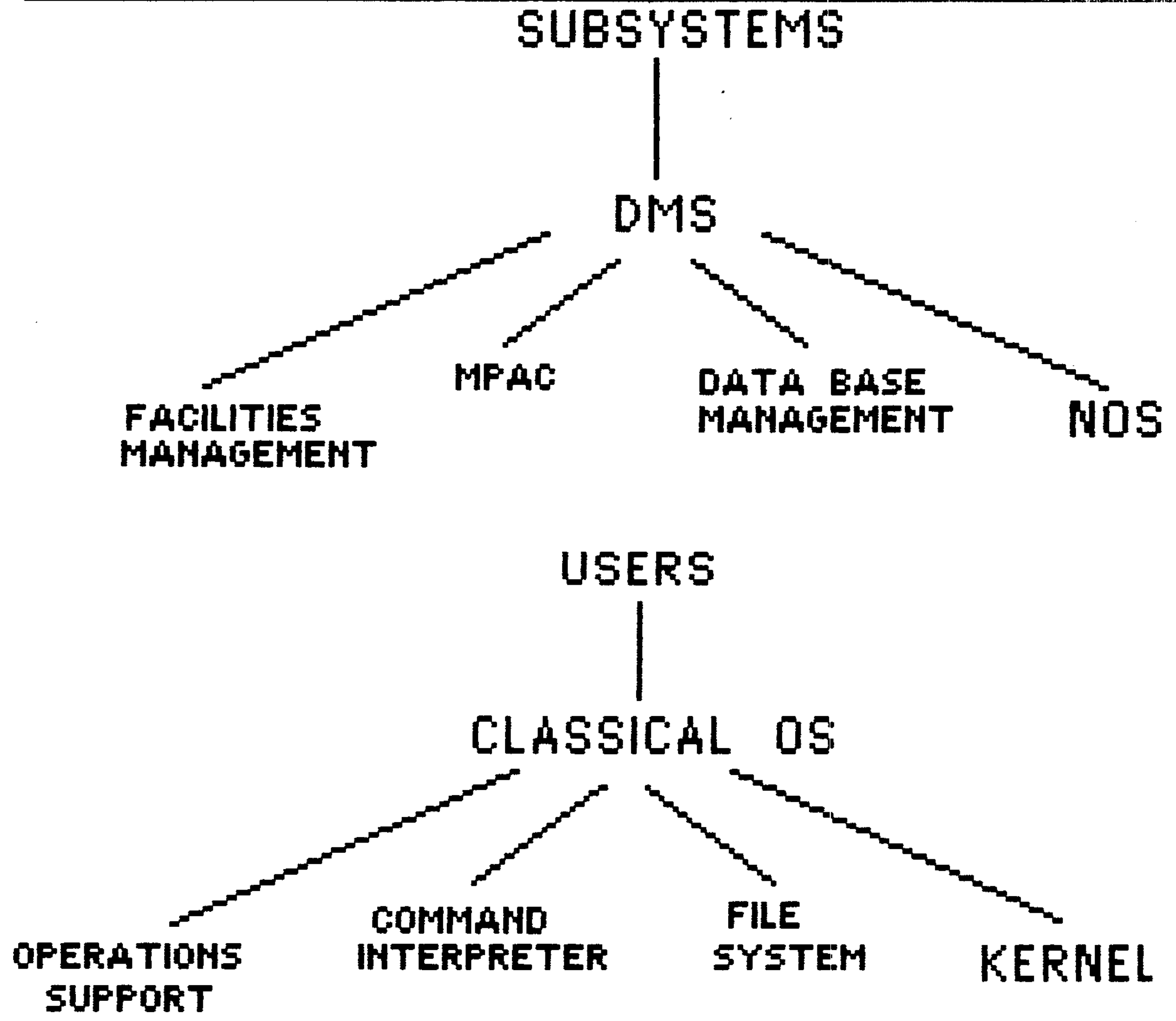
o HARDWARE/SOFTWARE FOR DMS TEST BED NETWORK TO SUPPORT NEAR TERM SYSTEM INTEGRATION ACTIVITIES

*PRINCIPAL ELEMENTS OF THE DMS

* NETWORK OF HARDWARE & SOFTWARE WHICH CONNECTS OTHER COMPUTER ELEMENTS AND SUPPORTS DATA EXCHANGE AND REMOTE CONTROL
* DATA BASE HARDWARE & SOFTWARE WHICH PROVIDES DATA STORAGE/RETRIEVAL SERVICES FOR SHARED DATA AND MANAGE CONCURRENCY ASPECTS OF DATA ACCESS
* MULTIPURPOSE APPLICATIONS CONSOLES (MPAC) TO PROVIDE UNIFORM MAN/MACHINE INTERFACES TO ALL FUNCTIONS
* FACILITIES MANAGEMENT HARDWARE/SOFTWARE TO PROVIDE SYSTEM-WIDE RESOURCE AND CONFIGURATION MANAGEMENT, ANALYSIS, AND SCHEDULING SERVICES

MODULAR DMS ORGANIZATION





PARALLELS BETWEEN DMS AND CLASSICAL OPERATING SYSTEMS

P.E. SOLLOCK

*CLASSICAL OPERATING SYSTEM ELEMENTS

* KERNEL--SET OF BASIC FUNCTIONS AND SERVICES UPON WHICH ALL SYSTEMS CAPABILITIES ARE ARE BASED
* FILE SYSTEM--PROVIDES A LOGICAL ORGANIZATION AND HIGH-LEVEL INTERFACE TO EXTERNALLY STORED DATA
* COMMAND INTERPRETER OR SHELL--PROVIDES AN INTERACTIVE MAN/MACHINE INTERFACE
* OPERATIONS SUPPORT--PROVIDES A SET OF UTILITIES WHICH CAN BE USED TO CONFIGURE, MANAGE, MONITOR AND OTHERWISE AID MANUAL OPERATION OF COMPUTATIONAL RESOURCES

*PRINCIPAL NOS FUNCTIONS

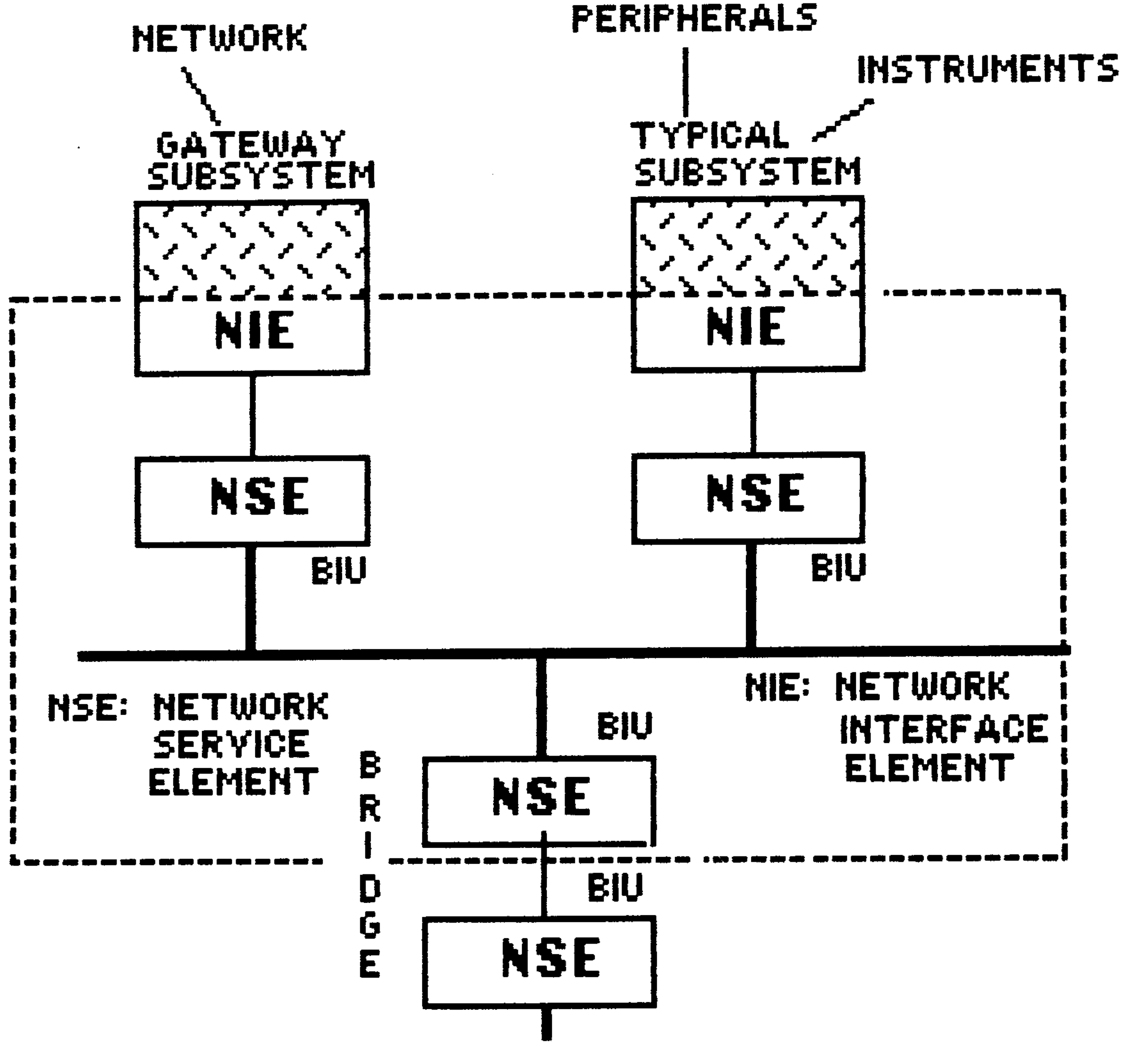
* CONTROL USE OF MEDIUM, INCLUDING ALL CONDITONS OF ACCESS, SUCH AS WHO, WHAT, WHEN AND FOR HOW LONG
* PROVIDES STANDARD APPLICATIONS-LEVEL COMMUNICATIONS INTERFACES FOR INTER-SUBSYSTEM TRANSACTIONS
* PROVIDE CONTINOUS OPERATION OF THE NETWORK INCLUDING GATHERING PERFORMANCE AND FAULT DATA, SUPPPORTING CONFIGURATION CHANGES, AND ERROR RECOVERY

NETWORK OPERATING SYSTEM DEFINITION AND DESIGN

AVIONICS SYSTEMS DIVISION

P.E. SOLLOCK

DOMAIN OF THE NOS



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Space Station Operations Language, Synopsis:

The Space Station Operations Language (SSOL) will serve a large community of diverse users dealing with the integration and checkout of Space Station modules. This briefing presents KSC's comprehensive plan to achieve Level A specification of the SSOL system, encompassing both the language and its automated support environment.

The SSOL concept has been formulated to improve integration and test processing in the Space Station era. The concept is not composed of a single element, restricted to language alone, but a collection of fundamental elements that span languages, operating systems, software development, software tools and several user classes.

The following approach outlines a thorough process that combines the benefits of rapid prototyping with a coordinated requirements gathering effort. The end result will be a Level A specification of the SSOL requirements.

KSC SPACE STATION OPERATIONS LANGUAGE (SSOL) ACTIVITIES

LARRY WILHELM, KSC

4-18-85

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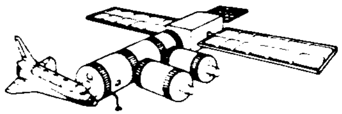
o **BACKGROUND:** THE CURRENT KSC INTEGRATION, TEST AND LAUNCH SYSTEMS FOR **SHUTTLE** ARE CUSTOM SOFTWARE DESIGNS, PREDOMINATELY ASSEMBLY LANGUAGE CODING AND REFLECT AN INVESTMENT TOTALING HUNDREDS OF MAN-YEARS.

o **PROBLEM:** THIS CUSTOM SYSTEM CONCEPT, COUPLED WITH DATED LAUNCH PROCESSING HARDWARE (CIRCA 1975), SEVERELY RESTRICTS THE APPLICATION OF TECHNOLOGICAL ADVANCES THAT COULD PRODUCE A LONG TERM COST SAVINGS OR ADDED DATA SYSTEM CAPABILITY.

IN THIS ENVIRONMENT, IT IS VERY DIFFICULT TO USE "OFF-THE-SHELF" HARDWARE (CPU'S), OPERATING SYSTEMS, DRIVERS, SHELLS, COMPILERS, AND IN SOME CASES, DEVELOPMENT TOOLS. PORTABILITY OF SYSTEM OR USER APPLICATION SOFTWARE IS RARE.

KSC SPACE STATION



FUTURE PROJECTS TECHNOLOGY

SPACE STATION OPERATIONS LANGUAGE (SSOL)

L. WILHELM

4-18-85

O **CHALLENGE:** TO DECREASE THE SPACE STATION INTEGRATION AND TEST SOFTWARE LIFE-CYCLE COST WHILE PROVIDING TECHNOLOGICAL TRANSPARENCY AND INCREASED I&T PROCESSING EFFICIENCY. THIS WOULD INCLUDE:

- CAPITALIZING ON THE COMMONALTY OF PROCESSING NEEDS (AND LANGUAGES) AT THE DEVELOPMENT, INTEGRATION AND LAUNCH SITES.
- IDENTIFYING AND USING STANDARDS IN SSOL INTERFACES, SUPPORT ENVIRONMENTS, DEVELOPMENT TOOLS AND LAYERS.
- FACILITATING TECHNOLOGICAL TRANSPARENCY BY PROMOTING THE THE USE OF MACHINE INDEPENDENT SOFTWARE AND HARDWARE IMPLEMENTATIONS.
- DEFINING EARLY SOFTWARE PORTABILITY GOALS FOR: USER APPLICATIONS, REAL TIME OPERATING SYSTEM S/W, LANGUAGE EXECUTORS AND DEVELOPMENT TOOLS

o **SSOL DEFINITION:** A USER ORIENTED SPACE STATION OPERATIONS LANGUAGE THAT IS:

- NEAR ENGLISH-LIKE AND SELF DOCUMENTING
- RELATIVELY TEST ARTICLE, INTERPRETER AND DATA BASE INDEPENDENT
- EXECUTABLE IN A REAL-TIME ENVIRONMENT AND CONTROLS USER INTEGRATION AND TEST PROCESSES
- AN EVOLUTION OF EARLIER, HIGH ORDER, PROCESS CONTROL LANGUAGES

o **SSOL SUPPORT ENVIRONMENT:** (KSC APPLICATION) THE NECESSARY ON-LINE AND OFF-LINE SOFTWARE SUPPORT ENVIRONMENT THAT FACILITATES SSOL LANGUAGE EXECUTION. INCLUDES THE OPERATING SYSTEM (NUCLEUS AND OS SUPPORT SOFTWARE), COMPILERS, EXECUTORS, CONFIGURATORS, SYSTEM-BUILD TOOLS, AND CONFIGURATION MANAGEMENT TOOLS.

O **NASA BENEFITS:** NASA WILL BENEFIT IN SPACE STATION INTEGRATION AND TEST PRODUCTIVITY IMPROVEMENTS BY THE REASONABLE APPLICATION OF SSOL CONCEPTS.

THE GOALS ARE:

- SIMPLER OPERATION AND DECREASED LIFE-CYCLE SOFTWARE COSTS
- REDUCTIONS IN THE REQUIRED DEGREE OF SPECIALIZATION IN HARDWARE, SOFTWARE, AND PEOPLE.
- BETTER LONG-TERM USE OF TECHNOLOGY, REDUCING NASA'S ONE-TIME DEVELOPMENT OR RE-HOSTING COSTS.
- GREATER REPEATABILITY OF I&T TEST ACTIVITIES BY THE USE OF TRANSPORTABLE USER APPLICATION PROGRAMS THAT FOLLOW THE TEST ARTICLE

SPACE STATION OPERATIONS LANGUAGE (SSOL)

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o **RELATED R&D EFFORTS:**

- JSC LEVEL C: SDE DEVELOPMENT, ON-BOARD SYSTEMS DEVELOPMENT INCLUDING THE EXECUTION OF HIGH ORDER LANGUAGES, UIL, AND I/F TO GROUND SYSTEMS
- GSFC: USER INTERFACE LANGUAGE DEVELOPMENT (UIL), STOL, TAE, PAYLOAD OPERATIONS SUPPORT
- UNIVERSITY OF COLORADO: USER INTERFACE LANGUAGE, PROCESS CONTROL TECHNIQUES.
- SSDS ARCHITECTURAL STUDY CONTRACTORS: SDE, SOFTWARE DEVELOPMENT, SYSTEM STANDARDS AND TOOLS
- VARIOUS GROUPS IN AI, EXPERT SYSTEMS, ADA AND MAN-MACHINE INTERFACES.

SPACE STATION OPERATIONS LANGUAGE (SSOL)

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O **KSC/SSOL TECHNICAL APPROACH:**

1. TO DEVELOP, DOCUMENT AND DEMONSTRATE A VIABLE SSOL LANGUAGE AND S/W SUPPORT ENVIRONMENT CONCEPT.
2. TO DEFINE A PROCESS FOR TECHNICAL INVOLVEMENT WITH KEY CENTERS, USERS AND DEVELOPERS WITHIN THE INTEGRATION AND TEST COMMUNITY.
3. TO PRODUCE A COORDINATED SSOL LEVEL A SPECIFICATION TO JSC LEVEL C.
4. TO VALIDATE AND REFINE THE CONCEPT IN A VAX-BASED R&D LABORATORY SETTING THAT FACILITATES TECHNICAL INFORMATION EXCHANGE.

KSC SPACE STATION FUTURE PROJECTS TECHNOLOGY

SPACE STATION OPERATIONS LANGUAGE

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O **THE SSOL CONCEPT FOCUSES ON:**

- PORTABILITY OF SYSTEM AND USER S/W WHERE FEASIBLE
- OPTIMAL USE OF COMMERCIAL S/W
- PROMOTION OF SYSTEM AND DEVELOPMENT S/W STANDARDS
- SUPPORT OF AN INTERPRETIVE EXECUTION MODE
- EXTENSIVE USE OF DATA BASES FOR: LANGUAGE INTERPRETATION, TEST ARTICLE DEFINITION, OFF-LINE PROCESSES
- INCLUSION OF SELECTED NEW TECHNOLOGY ADVANCES IN: AI, LANGUAGE DEVELOPMENT, TOOLS, AUTOMATION, GRAPHICS, WINDOWS AND ICONS

THE SSOL CONCEPT:

SPACE STATION OPERATIONS LANGUAGE (SSOL)

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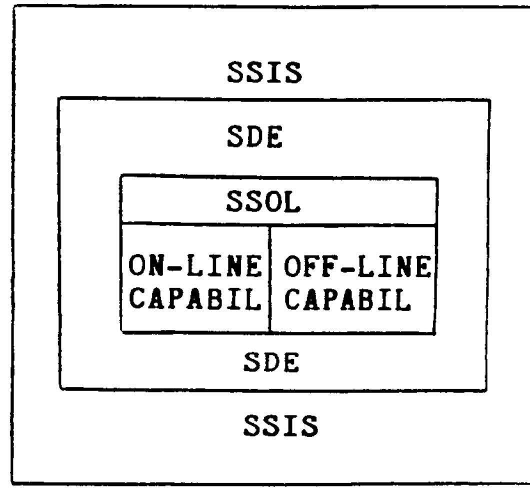
O **SSOL ENVIRONMENT AND INTERFACES:**

KSC TASKS:

- DEFINE USER REQUIREMENTS
- DEFINE SSOL FUNCTIONAL REQUIREMENTS
- DEFINE NON-SSOL FUNCTIONAL REQUIREMENTS
- DEFINE ON-LINE CAPABILITIES
- DEFINE OFF-LINE CAPABILITIES



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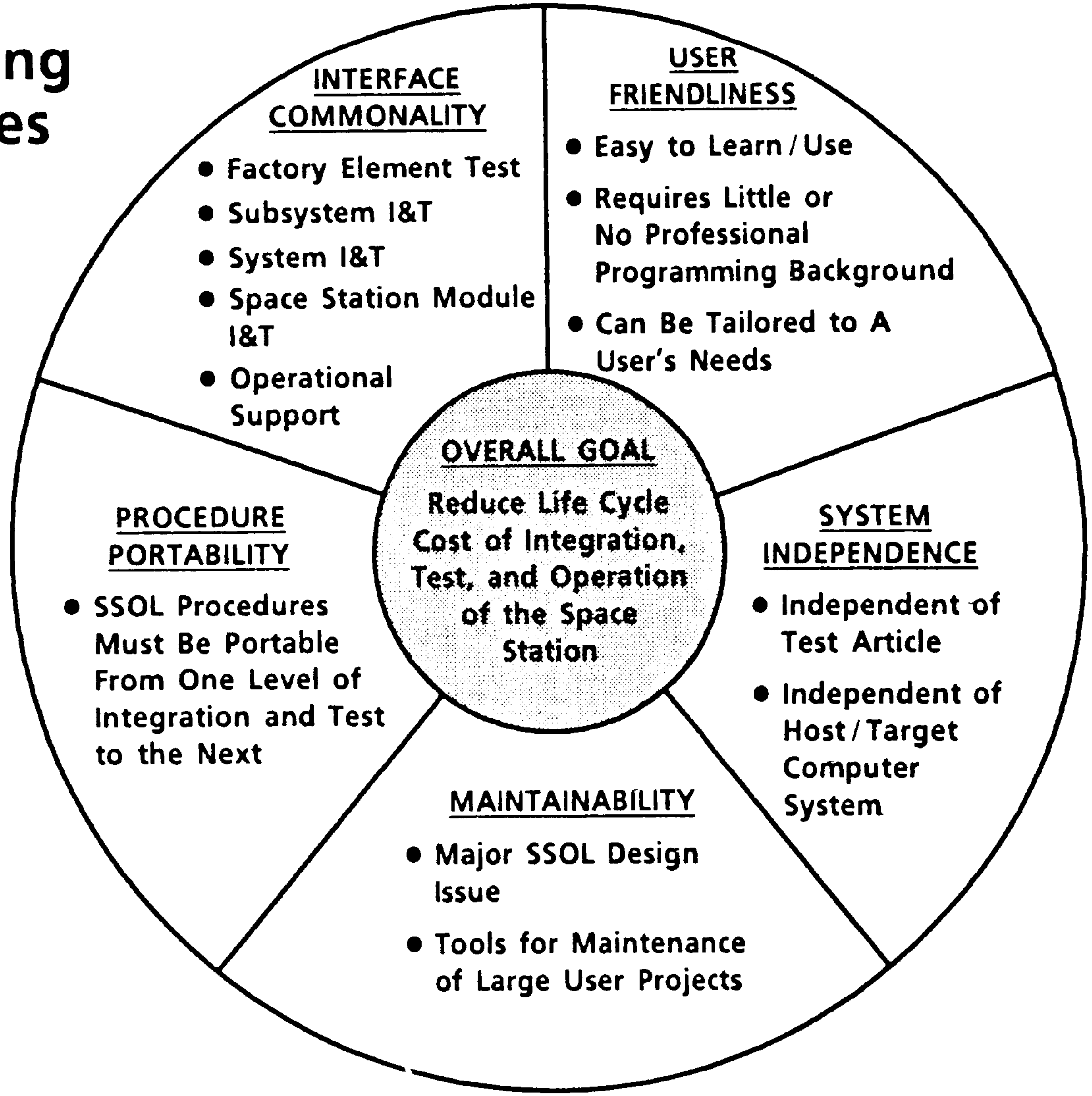
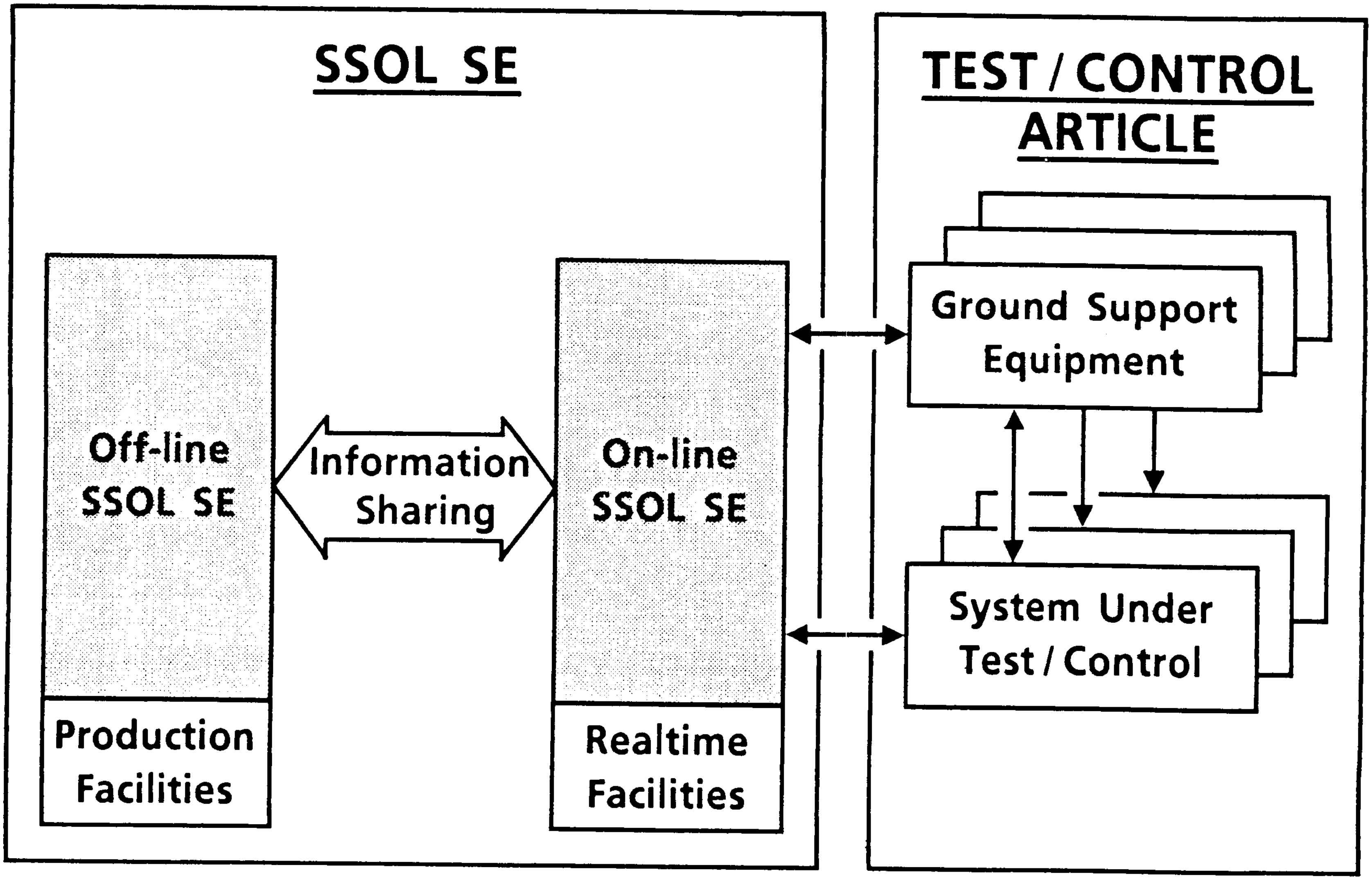
Architectural Goals and Objectives

- **Supporting Objectives**

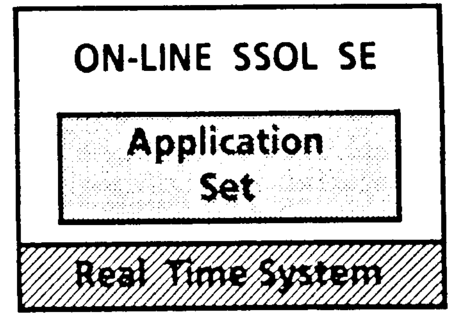


Top Level View of SSOL SE

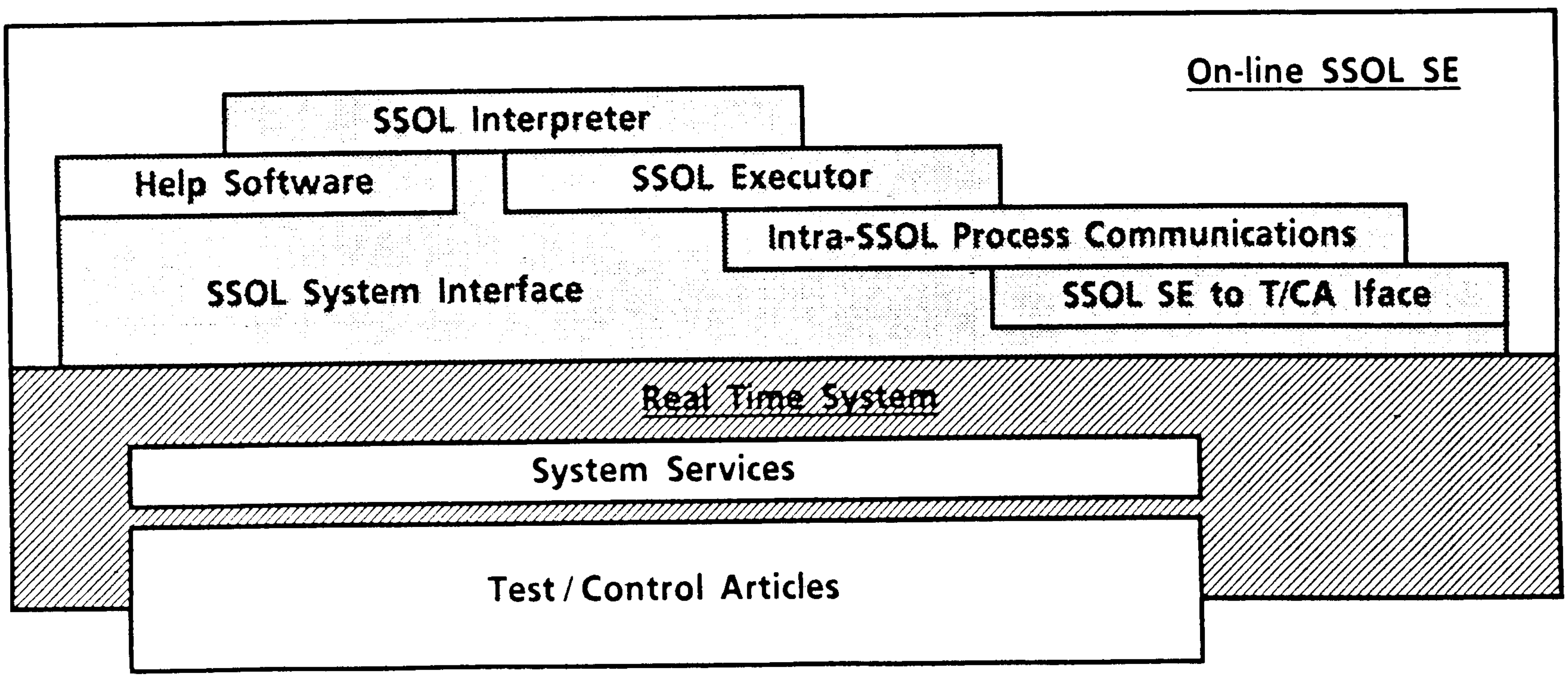


Overview of On-line SSOL SE

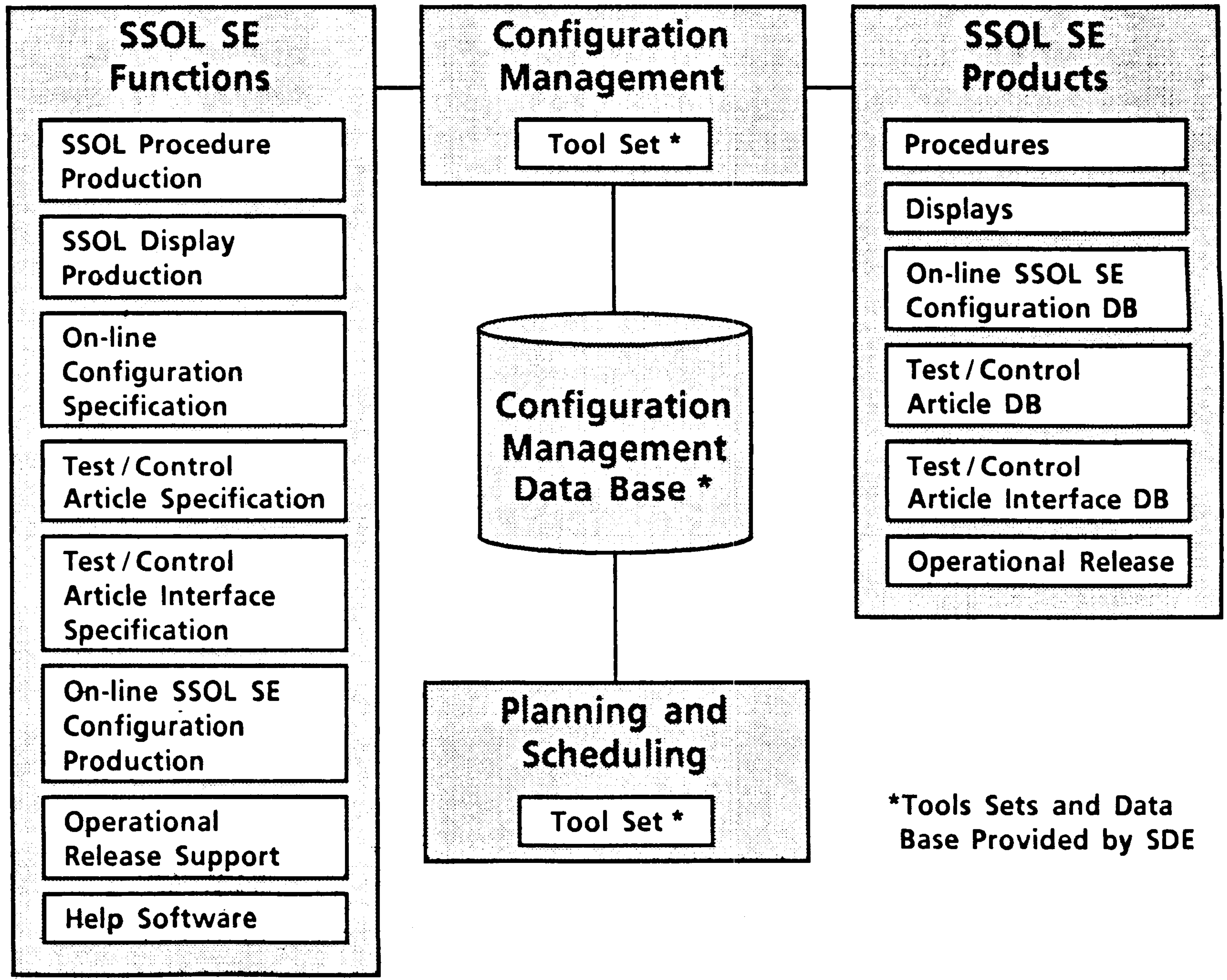
- Overall Organization:
  An Integrated Set of Application Programs



- Major Components and Relationships:



Overview of Off-line SSOL SE



THE SSOL DEFINITION PROCESS:

Documentation and End Products (KSC)

- SSOL Technical and Project Control Documentation

Planning Documentation

- POP Inputs
- KSC SSOL Plan
- Tri-Center Planning Package

Requirements and Conceptual Design Definition Documentation

- SSOL Requirements for I&T Community
- Integrated SSOL Requirements
- Assessments and Trades Report
- SSOL Level A Specification

SSOL Concept Evaluation Documentation and Products

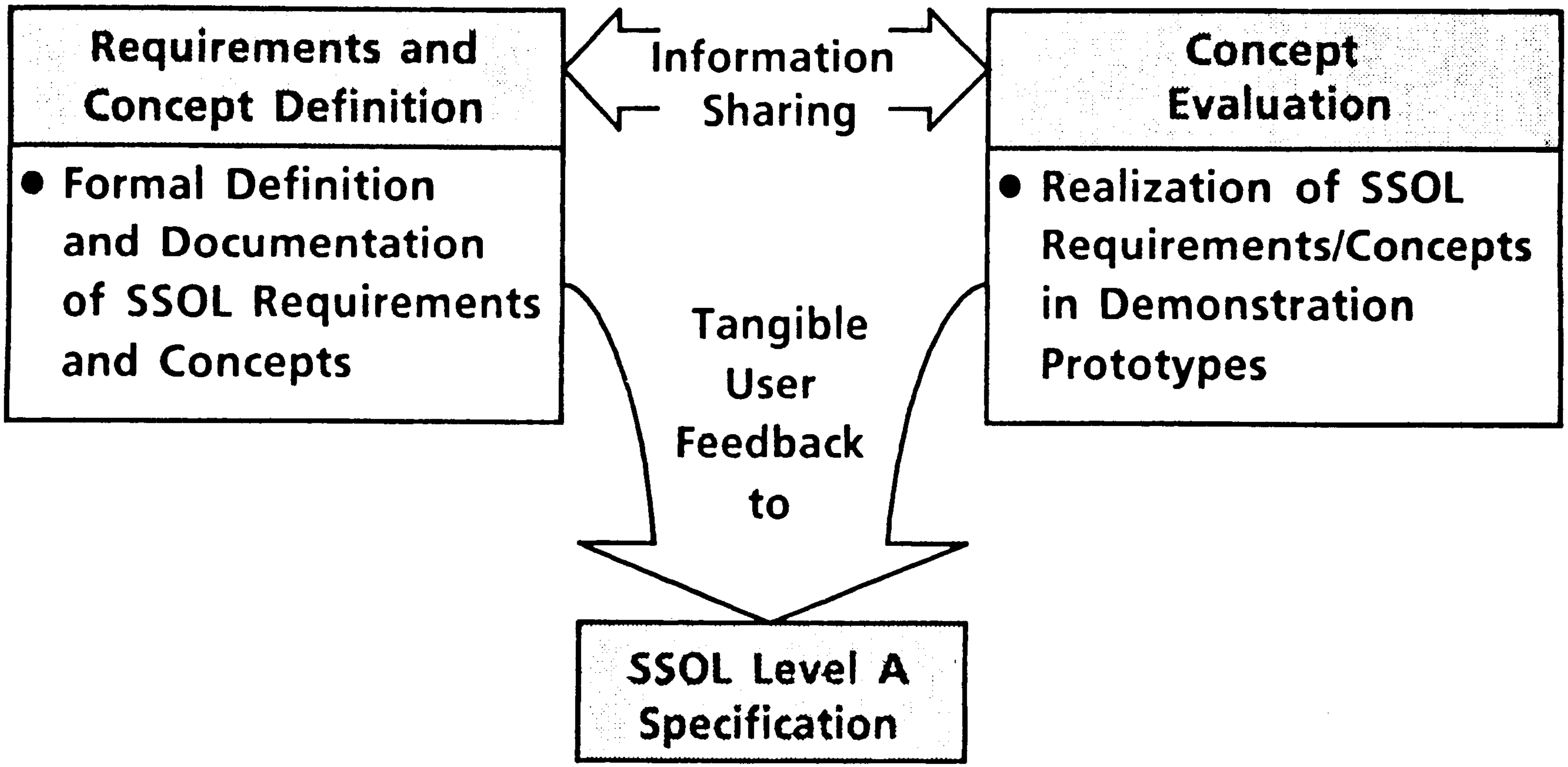
- Rapid Prototype Demonstrations
- Concept Evaluation Reports (2)

Internal KSC Documentation

- Working Papers
- Prototype Design Documentation
- Demonstration Scenarios
- T&E Reports
- Periodic Change Recommendations

KSC Approach

- Provides Concrete Evaluation, Validation, and Refinement of SSOL Requirements/Concepts



- Initial KSC Focus on Needs of I&T Community

C-5

THE SSOL DEVELOPMENT LABORATORY:

SPACE STATION OPERATIONS LANGUAGE
(SSOL)

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4-18-85

o **SSOL DEVELOPMENT LABORATORY:**

- VAX 11/780 BASED
- TWENTY-TWO MEMBER TEAM. JOINT CIVIL SERVICE AND CONTRACTOR.
- EMPLOYS RAPID PROTOTYPING: REQUIREMENTS-PROTOTYPE-DEMONSTRATE-UPDATE LOOP
- SOFTWARE INCLUDES:

    OPERATING SYSTEM (DEC VMS)

    DATA BASE (DATATRIEVE)

    LANGUAGE DEVELOPMENT S/W (TWS)

    GRAPHICS DEVELOPMENT S/W (PRECISION VISUALS AND DEC)

    MODELING SOFTWARE (ASPEN)

    EMULATION SOFTWARE (POLYGON-240)

    UNIX

    PASCAL

    ADA

SPACE STATION OPERATIONS LANGUAGE (SSOL)

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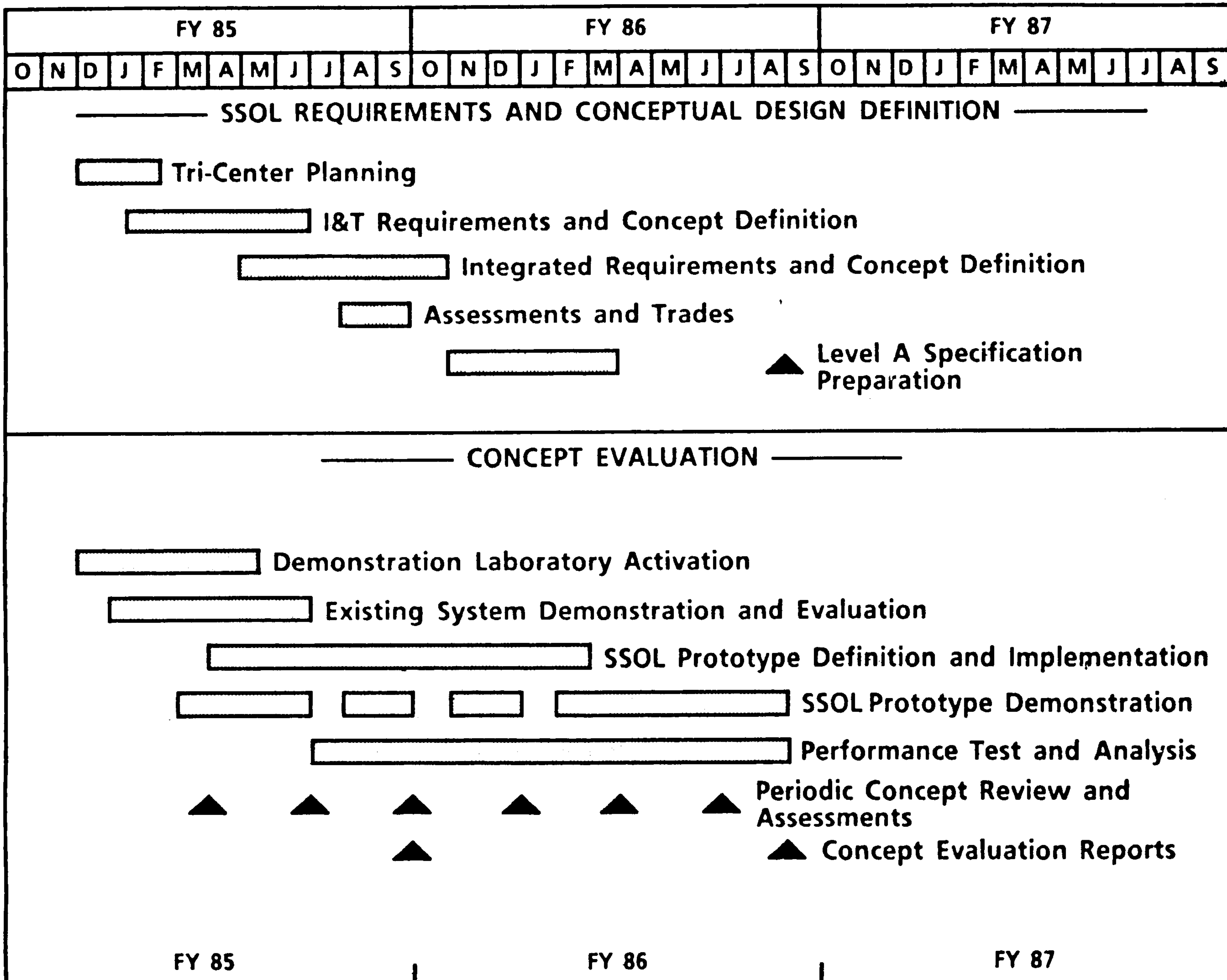
O **ACCOMPLISHMENTS:**

- CONCEPT DEVELOPMENT AND REQUIREMENT TEAMS ESTABLISHED
- KSC USER TEAM ESTABLISHED
- SSOL DEVELOPMENT LABORATORY ESTABLISHED
- DOCUMENTATION UNDERWAY: (NOT A COMPLETE LIST)

DOCUMENT:	STATUS:
KSC SSOL REQMTS. AND CONCEPT EVAL. PLAN	COMPLETE
TRI-CENTER PLAN	IN REVIEW
SSOL CONCEPT DOCUMENT	DRAFTED
SSOL SYSTEM REQUIREMENTS	IN WORK
SSOL PROTOTYPE DEFINITION DOCUMENT	IN REVIEW

Schedule



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CLOSING REMARKS

The agenda called for the Symposium to conclude with an open discussion of technology issues, problems, opportunities and/or directions as presented during the course of the three days of sessions. Ron Larsen (NASA HQ) led the wrap-up, first thanking everyone for taking the time to come to the Xerox Facility and for their excellent presentations. Excerpts from Mr. Larsen's remarks are paraphrased below. Other topics of discussion are presented as numbered items 1 through 4.

- This was the second symposium of its type sponsored by NASA-HQ and it used a different approach from that used at the conference held two years ago at the same Xerox facility. The emphasis in this conference was on minimal preparation of presentations, the information being non-review in nature, and focused primarily on OAST program participants.
- Although conferences are relatively expensive for all participants in terms of time and money, the consensus was that this symposium had done a good job in bringing together the research groups and the people who are managing/performing the programs in the agency. The conference provided a good mechanism to aid technology transfer and information exchange between centers. The mood of the participants was upbeat, supportive, and relaxed. Many people were able to get the telephone numbers and mail stop/codes of other participants working on related ideas.

1. The discussion provided numerous suggestions on how to improve the format of future conferences. Many participants felt that the mix of programmatic and technical talks was undesirable and that the agenda should have been better structured to budget specific times for both kinds of talks. It was suggested that half of the first day should be given over to purely programmatic talks and the rest of the conference devoted to technical presentations. Several people endorsed the idea that programmatic presentations were desirable in order to let the technical people working at other centers know what each center was working on. It was felt that this might encourage inter-center support of similar projects.

2. Some opinions were expressed to the effect that conferences for the Computer Science and Data Systems technologies were long overdue, but that perhaps it would be best to continue scheduling them two years apart rather than every year. Other opinions expressed: more deliberate opportunity for interaction should be available; the agenda should have less in the way of time constraints; limit the agenda in order to tighten the focus to more specific areas; have the participants provide handouts because it was difficult to see some of the viewgraphs even from the front row; and keep the conferences not too formal and not too loose.

3. Mr. Larsen also asked for feedback on whether or not the Washington area was the right place to hold these conferences. Suggestions for holding the next conference in the Bahamas, Santa Barbara, Hawaii, and Alaska were met with much enthusiasm, but the general feeling was that it wasn't as important as simply holding the conference in the first place. There was a suggestion that the conference should be rotated around the centers to give the technical people a chance to see the other centers.

4. Although the consensus was that the format provided a good structure for the conference, several suggestions were made on how to improve it for future conferences. The location of the next conference was left up to NASA HQ, with the general feeling that it was not that important. On the whole, the 1985 Computer Science and Data Systems Technical Symposium went smoothly and the conference met its objective as a forum for the exchange of technical information among those working in the technologies.

N87-29169

SYSTEMS ANALYSIS METHODOLOGY FOR LARGE SCALE SYSTEMS

TASK MANAGER: KAREN L. MOE
GSFC CODE 522.2
RTOP NO. 506-58-16

THE OBJECTIVE OF THIS TASK IS TO DEVELOP A SYSTEMATIC APPROACH OR METHODOLOGIES FOR DEFINING AND EVALUATING ALTERNATIVE STRATEGIES FOR DEVELOPING DATA PROCESSING AND MANAGEMENT SYSTEMS. VARIOUS TECHNIQUES AND SYSTEM ENGINEERING TOOLS SUCH AS N-SQUARED INTERFACE CHARTS, FUNCTIONAL DECOMPOSITION TREES, SYSTEM MODELS, DE MARCO DIAGRAMS, ETC., ARE INTEGRATED TO DEVELOP AND PRESENT TO THE ANALYSTS AND USERS AN EARLY DEFINITION OF SERVICES DESIRED ALONG WITH PROBABLE AND COMPATIBLE OPERATIONS CONCEPTS. IN ADDITION, THE OUTPUTS OF THESE INVESTIGATIONS CAN IDENTIFY, EARLY ON, POTENTIAL DATA MANAGEMENT ISSUES, KEY SETS OF DATA CHARACTERISTICS, PREVIOUS APPROACHES THAT WERE EFFECTIVE, AND ANY NEW TECHNOLOGIES THAT MAY BE BENEFICIAL TO EXPLORE. AN IMPORTANT GUIDELINE RESULTING FROM THIS INTEGRATED EFFORT IS TO IDENTIFY PERFORMANCE DRIVERS AND TRADEOFFS NECESSARY FOR A SPECIFIC DEVELOPMENT EFFORT. THESE METHODOLOGIES ARE PLANNED TO BE ASSESSED BY APPLYING THEM TO MISSIONS SUCH AS UARS, HITCHHIKER-G, EARTH OBSERVATION SYSTEM, AND SPACE STATION PAYLOAD OPERATIONS.

SYSTEM ANALYSIS METHODOLOGY FOR LARGE SCALE SYSTEMS

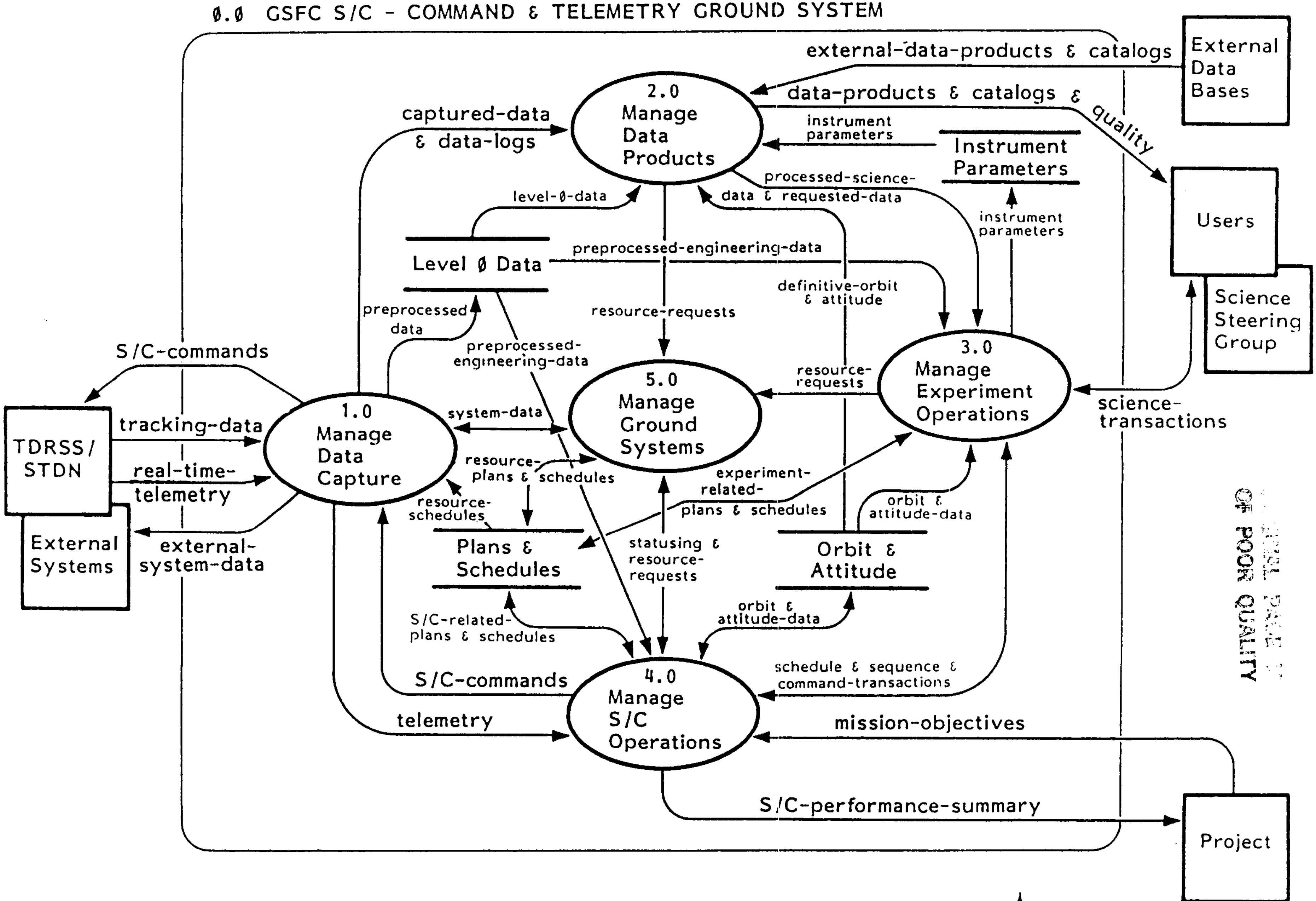
OBJECTIVE

- o DEVELOP METHODOLOGIES FOR GENERATING AND ASSESSING
  - ALTERNATIVE DATA MANAGEMENT/HANDLING SYSTEMS
  - MISSION OPERATIONS CONCEPTS

APPROACH AND PRODUCTS

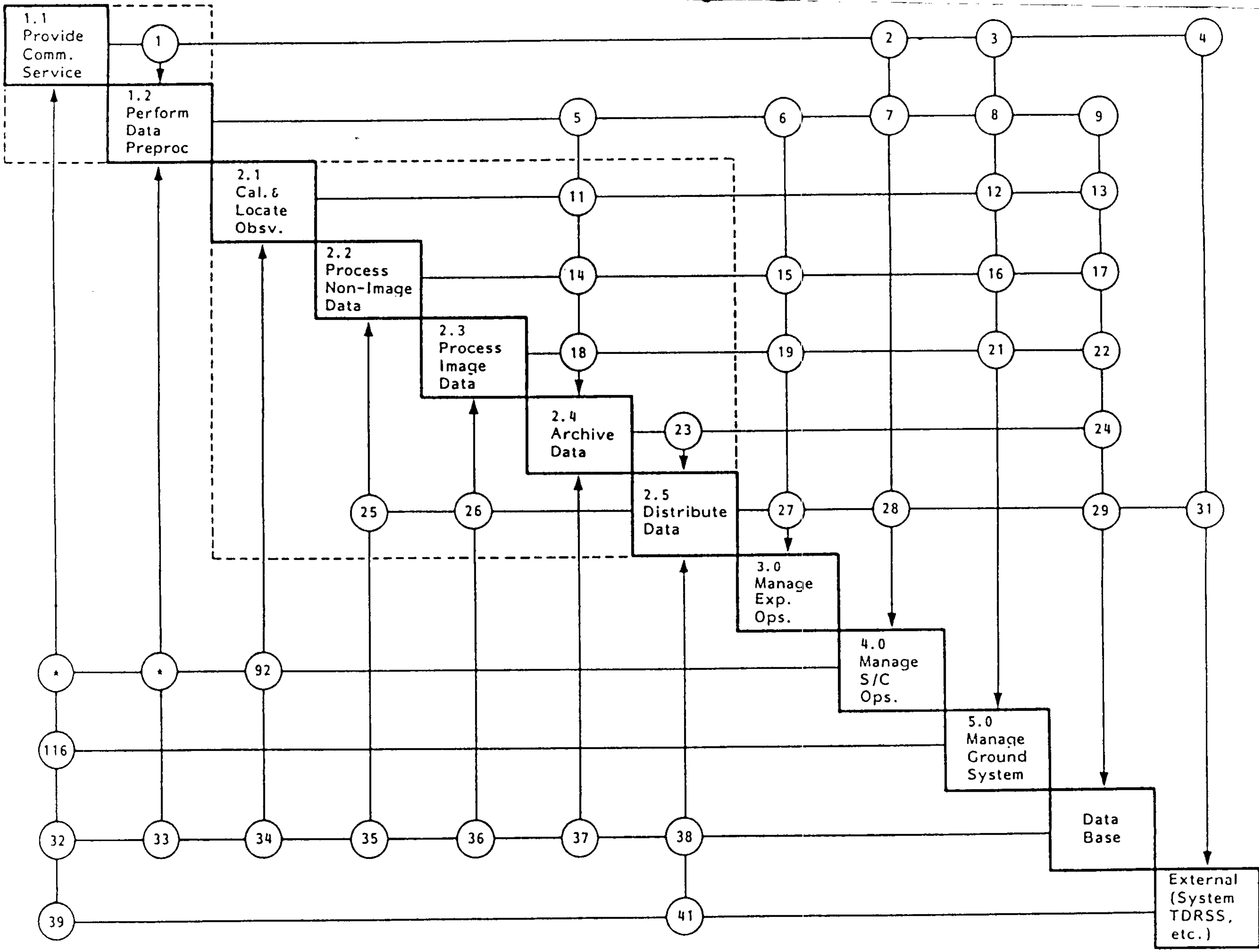
- o DEVELOP SYSTEM ENGINEERING "TOOL KIT"
  - GENERATE GENERIC SYSTEM FUNCTIONAL MODEL '84
  - DEVELOP REFERENCE DATA BASE '85-'85
    DATA SET CHARACTERISTICS
    EXPERIENCE WITH PAST MISSIONS
    NEW TECHNOLOGIES
    POTENTIAL DATA MANAGEMENT ISSUES
- o DEVELOP AND EVALUATE METHODOLOGY
  - DEVELOP SYSTEMATIC APPROACH TO DEFINING
    DATA MANAGEMENT SYSTEM ANALYSIS METHODOLOGY '84
    MISSION OPERATIONS CONCEPT '84
  - DESIGN AND DEVELOP COMPUTER TOOL '85-'86
    TO AID INTEGRATION OF METHODOLOGY STEPS
  - APPLY METHODOLOGY TO MISSIONS (UARS, HITCHHIKER-G, SPACE STATION PAYLOAD OPERATIONS, EOS) '85-'86

Ø.Ø GSFC S/C - COMMAND & TELEMETRY GROUND SYSTEM



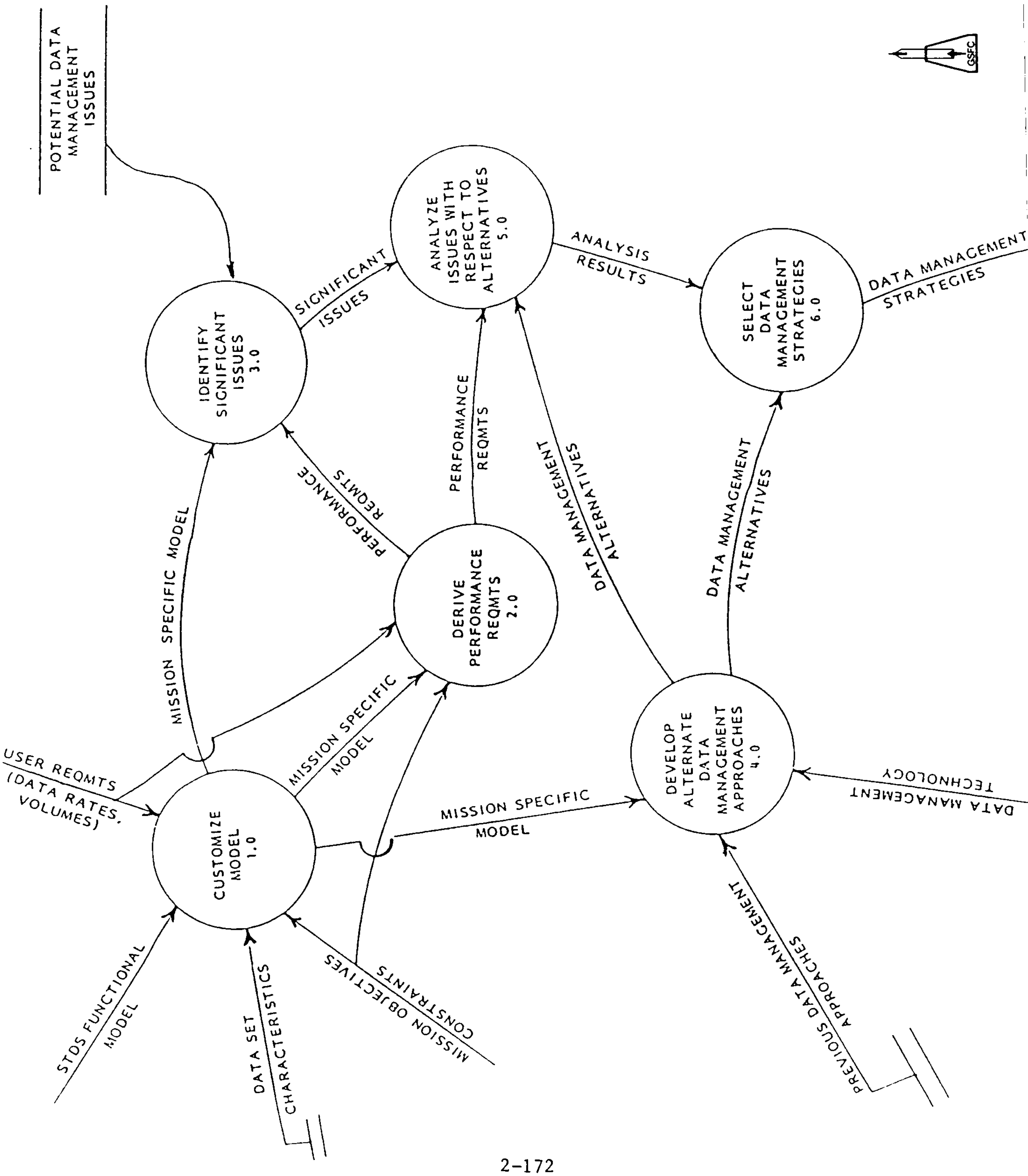
- MANAGE DATA PRODUCTS (2.0)
  - CALIBRATE & LOCATE OBSERVATION (2.1)
    - CALIBRATE OBSERVATION (2.1.1)
    - LOCATE OBSERVATION (2.1.2)
  - PROCESS NON-IMAGE DATA (2.2)
    - ENGINEERING UNIT CONVERSION (2.2.1)
    - COMBINE INSTRUMENT DATA (2.2.2)
  - PROCESS IMAGE DATA (2.3)
    - CALCULATE GEOMETRIC TRANSFORMATION (2.3.1)
    - IMAGE RESAMPLING (2.3.2)
    - IMAGE ENHANCEMENT (2.3.3)
  - ARCHIVE SCIENCE DATA (2.4)
    - ARCHIVE DATA (2.4.1)
    - ASSESS DATA QUALITY (2.4.2)
    - GENERATE DATA CATALOG/DIRECTORY (2.4.3)
  - DISTRIBUTE DATA (2.5)
    - ACCESS DATA (2.5.1)
    - MAINTAIN/UPDATE DATA CATALOG/DIRECTORY (2.5.2)
    - DISTRIBUTE DATA (2.5.3)

FIGURE A-2. MANAGE DATA PRODUCTS FUNCTION (2.0) TREES



* See N^2 Chart for Producing Function

FIGURE 7-1 N^2 Relationship for Functions 1.0 and 2.0

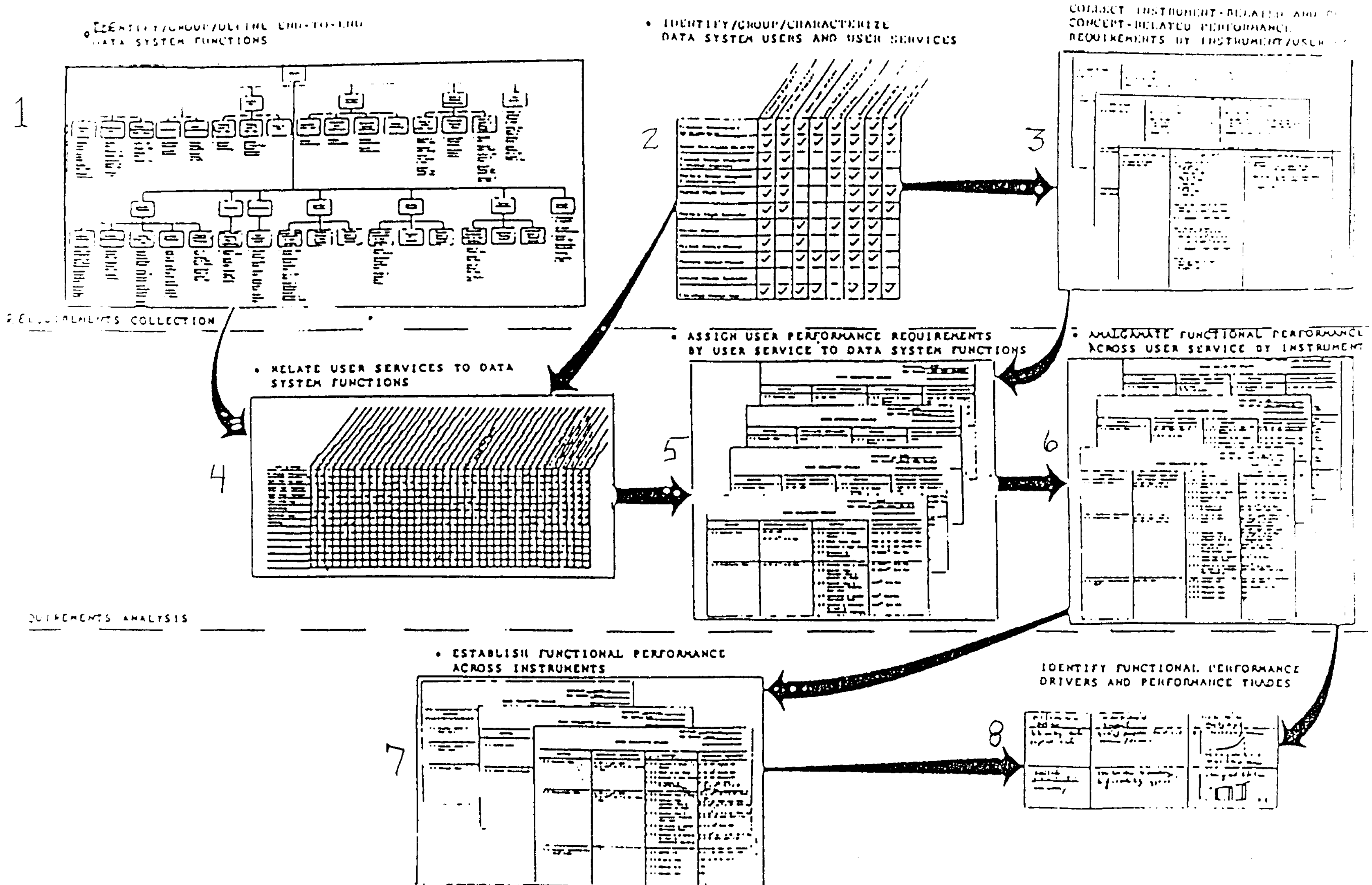

POTENTIAL DATA MANAGEMENT ISSUES
IDENTIFY SIGNIFICANT ISSUES 3.0
SIGNIFICANT ISSUES
ANALYZE ISSUES WITH RESPECT TO ALTERNATIVES 5.0
ANALYSIS RESULTS
SELECT DATA MANAGEMENT STRATEGIES 6.0
DATA MANAGEMENT STRATEGIES
PERFORMANCE REQMTS
PERFORMANCE REQMTS
DATA MANAGEMENT ALTERNATIVES
DATA MANAGEMENT ALTERNATIVES
MISSION SPECIFIC MODEL
DERIVE PERFORMANCE REQMTS 2.0
MISSION SPECIFIC MODEL
USER REQMTS (DATA RATES, VOLUMES)
CUSTOMIZE MODEL 1.0
MISSION SPECIFIC MODEL
DEVELOP ALTERNATE DATA MANAGEMENT APPROACHES 4.0
DATA MANAGEMENT TECHNOLOGY
STDS FUNCTIONAL MODEL
DATA SET CHARACTERISTICS
MISSION OBJECTIVES
CONSTRAINTS
PREVIOUS DATA MANAGEMENT APPROACHES
GSFC

FUNCTIONAL PERFORMANCE REQUIREMENTS METHODOLOGY

- o REQUIREMENTS COLLECTION
  1. IDENTIFY, GROUP & DESCRIBE END-TO-END DATA SYSTEM FUNCTIONS
  2. IDENTIFY, GROUP & CHARACTERIZE DATA SYSTEM USERS AND USER SERVICES
  3. COLLECT INSTRUMENT-RELATED, OPERATIONS-RELATED PERFORMANCE REQUIREMENTS BY INSTRUMENT/USER PAIR

- o REQUIREMENTS ANALYSIS
  4. RELATE USER SERVICES TO DATA SYSTEM FUNCTIONS
  5. ASSIGN USER PERFORMANCE REQUIREMENTS BY USER SERVICE TO DATA SYSTEM FUNCTIONS
  6. AMALGAMATE FUNCTIONAL PERFORMANCE ACROSS USER SERVICE BY INSTRUMENT

- o REQUIREMENTS SPECIFICATION
  7. ESTABLISH FUNCTIONAL PERFORMANCE ACROSS INSTRUMENTS
  8. IDENTIFY FUNCTIONAL PERFORMANCE DRIVERS AND TRADE-OFFS



FUNCTIONAL PERFORMANCE REQUIREMENTS METHODOLOGY

SYSTEMS ANALYSIS METHODOLOGY FOR LARGE SCALE SYSTEMS

NEXT STEP - APPLICATION TO EARTH OBSERVATION SYSTEM (EOS)

- o CHALLENGE
  - STUDIES IN EARTH SCIENCE REQUIRE ANALYTIC AND CORRELATIVE STUDIES OF DATA FROM PAST, PRESENT AND FUTURE MISSIONS. DATA PREPROCESSING AND DELIVERY, DATA ARCHIVING, SCIENCE PROCESSING, AND AUTOMATED DATA COLLECTION/LOCATION (ADCLS) ARE KEY ELEMENTS OF EOS.

- o APPROACH
  - DEVELOP PROTOTYPE COMPUTER TOOL (PC TYPE DATABASE & SPREADSHEET), TEST USING UARS DATA
  - CONDUCT SURVEY OF GSFC SCIENTISTS FOR MOST LIKELY EOS INSTRUMENTS (E.G., LASA, HMMR, MODIS) TO IDENTIFY

    ANTICIPATED EOS USER COMMUNITY
    SERVICES EXPECTED
    GENERIC FUNCTIONS REQUIRED TO PROVIDE SERVICES
    GENERIC PERFORMANCE ATTRIBUTES OF SERVICES
    (DEVELOP USER SERVICE VS. PERFORMANCE MATRIX)
  - IDENTIFY CRITICAL PERFORMANCE DRIVERS AND TRADEOFFS

Computer Science and Data Systems Symposium

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	Rousey, William	(818) 354-8026	JPL MS 161-137
	Solomon, Jerry	(818) 354-2722	JPL MS 168-514
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	Foudriat, Ed	(804) 865-2077	MS 152
	Eckhardt, Dave	(804) 865-3681	MS 130
	Murray, Nick	(804) 865-3535	MS 473
	Hendricks, Herb	(804) 865-3777	MS 473
	Benz, Harry	(804) 865-3535	MS 473
	Hatfield, Jack	(804) 865-2171	MS 494
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